MULTIPROGRAMMER

MODEL 6940B

OPERATING AND SERVICE MANUAL

FOR SERIALS 1923A-03311 AND ABOVE *

* For Serials above 1923A-03311
a change page may be included.

HP Part No. 06940-90007
Microfiche Part No. 06940-90008

Printed: June, 1979

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

SECTION I
GENERAL INFORMATION

1-1 SCOPE

1-2 This instruction manual provides complete operating and service instructions for the 6940B Multiprogrammer. Accessory input/output cards and the 6941B Multiprogrammer Extender, which are usually combined with the 6940B in a Multiprogrammer System, are covered in separate instruction manuals. However, in order to present overall system concepts, this instruction manual also covers system installation and operating considerations as well as brief physical and functional descriptions of the 6941B and the accessory input/output cards.

1-3 DESCRIPTION

1-4 The 6940B Multiprogrammer is the master control unit for bidirectional (i. e. output data distribution/input data multiplexing) Multiprogrammer Systems. The 6940B can be used in a single-unit system employing from one to fifteen plug-in input/output cards, or in a multi-unit system consisting of one 6940B master unit and up to fifteen 6941B extender units. Each extender unit can also accomodate up to fifteen input/output cards, allowing a multiprogrammer system to be modularly expanded up to a maximum of 240 input/output channels. Hence, the multiprogrammer system can be used to convert a single computer I/O channel into a total of 240 I/O channels.

1-5 SYSTEM CONFIGURATION

1-6 A typical system configuration is shown pictorially in Figure 1-1. The multiprogrammer system is controlled by a digital computer which supplies 16-bit binary words to: (1) control the mode of operation of the system (for instance, to allow the multiprogrammer to time share input and output functions; to establish timing synchronization between the computer and I/O devices through the multiprogrammer etc.); (2) address output cards and supply the output quantity, in binary-encoded form, to be developed by the output cards for application to the output device; and (3) address input cards for the reception of binary-encoded input data. Brief physical and functional descriptions of the three system components (the 6940B, input/output cards, and 6941B) are given in the following paragraphs. A detailed functional description of the 6940B Multiprogrammer is provided in Section IV.

1-7 6940B Multiprogrammer

1-8 The 6940B Multiprogrammer mainframe consists of a hinged front control panel, a 20 position card cage, a main dc power supply, and a rear panel containing input and output data and ac power connectors. Of the 20 card positions, 4 (slots 100, 200, 300, and 500) contain interfacing, data processing, and control cards supplied with the mainframe, and 15 (slots 400 through 414) house accessory input/output cards. Slot 600 is reserved for a voltage regulator card which is required for use with D/A voltage converter and current controller output cards. Unused input/output card slots (400 series) or slot 600 can be left empty.

1-9 Data and control signals are exchanged between the computer and multiprogrammer through connector J1 on the rear panel of the 6940B. Computer inputs (16 data bit lines and a control gate line) to the multiprogrammer are routed through adapter card A7 to the back-plane wiring of interconnect board A9. Input card A1 (slot 100) is the first plug-in card to receive the inputs. A standard A1 input card is supplied with all 6940B Multiprogrammers and provides the proper termination for digital data sources employing TTL or DTL microcircuit logic output drivers having ground-true logic levels (logical 1 = LO; logical 0 = HI).

1-10 Multiprogrammer outputs to the computer (16 data lines and a control flag line) are also applied to connector J1 through adapter card A7. The outputs are applied to A7 from the back-plane wiring of interconnect board A9. The data bit lines are driven by microcircuit output drivers located on the A3 plug-in board (bits 0-11) and the A2 plug-in board (bit 15). The data bit drivers produce ground-true logic levels compatible with systems employing either TTL/DTL logic circuits or, at the option of the user, with systems requiring higher logic level inputs. Note that the multiprogrammer flag output is produced by a microcircuit driver on the A2 board but that it is terminated on the A1 input board and provides only ground-true TTL/DTL compatible logic levels. The optional A1 input board must be used for the flag output (as it is for the computer data and gate inputs) if alternate logic levels are desired.

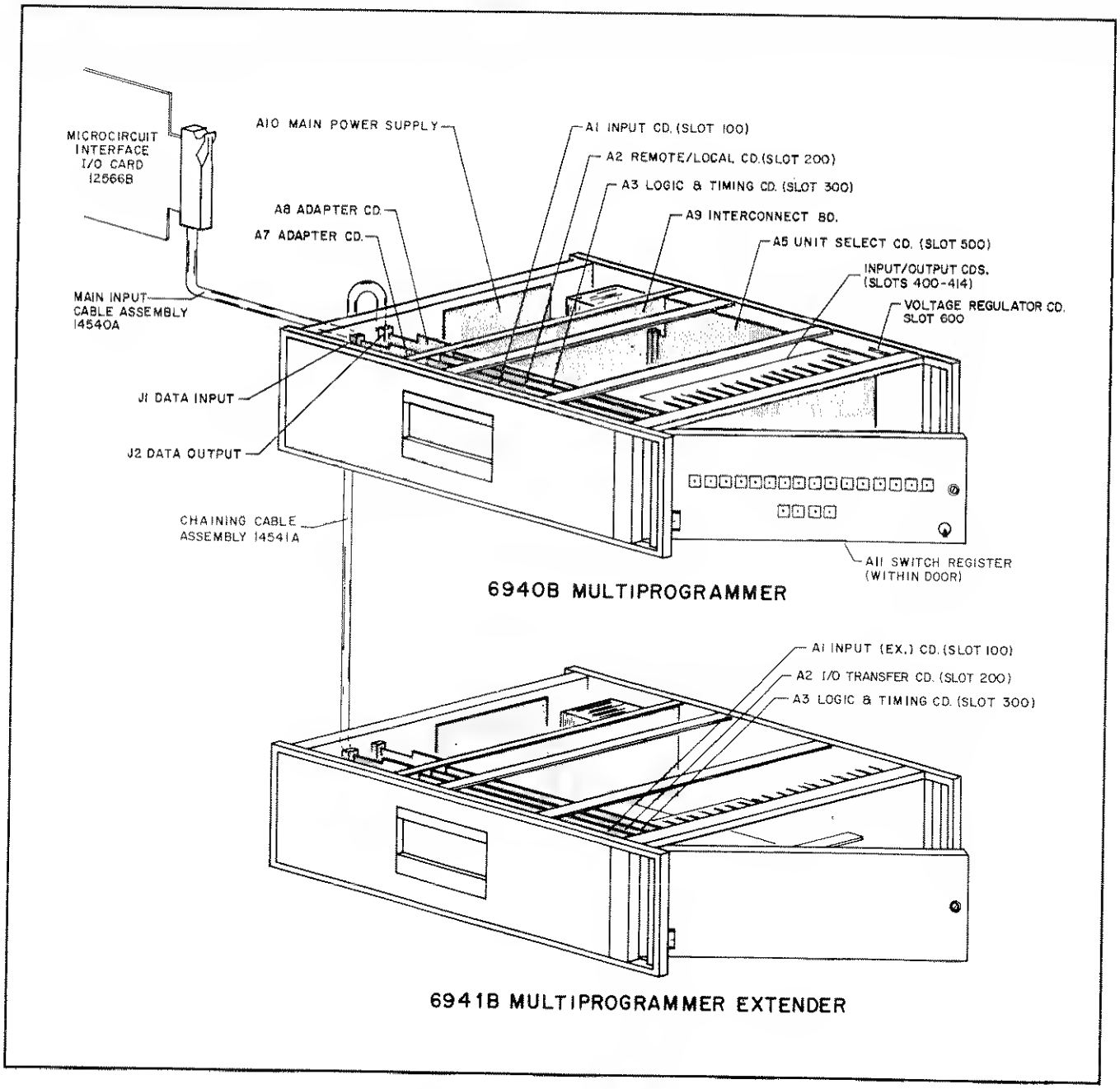


Figure 1-1. System Configuration

1-11 After being properly interfaced, the computer inputs are applied to remote/local card A2, in slot 200. The remote/local card selects either the computer or the local control panel as the programming source and distributes the data to the A3 logic and timing card. In addition, the A2 board distributes bits 12-15 (which contain an address for all programmed words received from the programming source) to the control panel for display. The A2 card also receives bits 0-11 from the A3 card. These bits are either the original programming source bits or are input bits from a multiprogrammer input card depending on the mode of operation in which the multiprogrammer is placed. Bits 0-11 are also applied to the control panel for display.

1-12 In addition to remote/local data selection and data distribution, the A2 card also processes data bit 15 in conjunction with an input request identification control signal which is common to all input cards. If the input mode is selected, the request signal is combined with bit 15 such that the logic sense of bit 15 reflects the data readiness status of an input card. If the input mode is *not* selected, bit 15 reflects the logic sense of bit 15 supplied by the selected programming

source. Notice that this processed bit 15 output is *not* the same bit 15 output supplied to the A3 logic and timing card (the A3 card receives the programming source bit 15). Instead, the processed bit 15 output of A2 is applied to the A9 card where it is jumpered for output to the computer via connector J1 as previously described. Note that the multiprogrammer also sends data bits 0-11 to the computer. If the input mode is not selected, bits 0-11 represent bits 0-11 received from the computer. If the input mode is selected, bits 0-11 represent data from an input card.

1-13 The A3 logic and timing card has three main functions. First, the A3 card provides buffer amplification for the remote/local programmed address and data bits received from the A2 card. After buffering, address bits 12-15 are distributed without further processing to unit select card A5 where they are used in processing programmed control words. The address bits are also distributed to all input/output card slots in this unit and all extender units. The card slots in each unit are program-selected by the address bits which are encoded with a unique combination associated with each card slot.

1-14 The second function performed by the A3 card involves the selection of programmed data bits versus input data bits. The A3 card selects (after buffering) programmed data bits 0-11 from the A2 card if the multiprogrammer is *not* in the input mode. Assuming the multiprogrammer has not been placed in the input mode, the programmed data bits are applied to unit select card A5 where, if address bits 12-15 identify the programmed data as a control word, control mode and unit select data contained in the control word data bits are stored and processed. The selected programmed data bits are also applied to the multiprogrammer output card slots where they are used if the associated address bits contain the card slot address. Note that the programmed data bits, like the address bits, are also distributed to all extender unit output card slots. If the multiprogrammer is in the input mode, the A3 card selects input data bits 0-11 from an addressed input card. The data bit outputs of all input cards of every multiprogrammer unit in the system are combined in a common data bus (which is, in fact, common to the output card data bits) with only the addressed input card supplying the input data to the A3 card selection circuits. After selecting either programmed data or input data bits, the selected data is also buffered on the A3 card from which they are applied to the A9 card where they are jumpered and routed to the J1 connector for output to the computer along with address bit 15, as previously described.

1-15 The third function performed by the A3 card is the generation of the multiprogrammer flag signal for output to the programming source. The flag notifies the programming source whether the multiprogrammer system is busy processing the last programmed task or if it is ready for the next one.

1-16 Unit select card A5 examines specific bits of the programmed data to determine if the data represents a control word or a data/address word. The definitions and functions of control, data, and address words are covered in detail in Sections III and IV. In general, a control word is issued to select a unit in the system to receive data during output modes or to transmit data back to the computer during input modes. The data word contains the address of 1 to 15 possible output card slots in the selected unit and the data to be entered into the addressed output card. Similarly, the address word contains the address of 1 of 15 possible input card slots in the selected unit. The data is returned to the computer from the addressed input card.

1-17 If the unit select card determines that the programmed word is a control word, it decodes and stores the unit selection. The unit selection enables the output cards of the selected unit to receive address and data information contained in the next programmed data word. Of course, the unit selection also enables the input cards of the selected unit to receive the address information contained in the next programmed address word thereby allowing the card to input its data. The 6940B is assigned unit number Ø0 (UØØ); extender units are numbered UØ1 through U15, with UØ1 being the first and U15 the last in the chain. Note that addressing is accomplished in two steps. The unit is first selected as part of a control word. Next, either the particular output card address and associated data are issued together as a data word or an input card address is issued in an address word. A unit selection remains in effect until a new unit is selected by a later control word. This permits all input/output cards of a selected unit to be addressed without the need to repeat the unit address.

1-18 The buffered data and address bits, 15 unit selection lines, and mode control and timing signals are conveyed to output connector J2 by adapter card A8. A chaining cable is then connected from output connector J2 of the 6940B to input connector J1 of the first 6941B extender unit in the system. In the other direction, the input data bits and extender unit control signals are received at connector J2 from the first 6941B extender unit in the system.

1-19 Input/Output Cards

1-20 The function of the output cards is to develop an output quantity proportional to programmed data, and to deliver this quantity to the user's system. The output cards are similar to one another in that each contains address gate, data storage, and output data conversion circuits. The nature of the output conversion circuits determines the card type.

1-21 Output cards are programmed using a 16-bit data word. Twelve of the bits represent programmed data while the remaining four bits contain the output card slot address. The 12 bits are used in different ways on the various type output cards to develop an output to the user's systems. For digital-type output cards, the 12-output bits can be either logic levels or contact closures. For analog-type output cards (resistance, voltage, or current) the data bits are used to control a D/A converter. For resistance output cards, the D/A converter is a binary-weighted precision resistance network. The variable resistance output of these cards can be used to program an external power supply or other device that can be programmed by a variable resistance. For voltage and current-type output cards, the D/A converter is a DAC module which generates a bi-directional binary-weighted output current. Operational amplifiers on the cards receive this current and convert it to a proportional bi-directional voltage or higher magnitude bi-directional current.

1-22 An output card programmed to a particular output value will hold that value until it is readdressed and the programmed data is changed.

1-23 The function of the input cards is to receive data from the user's system and make it available to the computer. The input cards each contain an address gate and input data interface circuits. Further, input cards can be supplied with storage capability so that the user's system need supply input data for a short period of time after which it is maintained in the input card until accepted by the computer. The nature of the user's input; i.e., digital input data versus relay contact closure data, determines the card type.

1-24 Input cards are programmed using a 16-bit address word. The same four bits used to specify an output card slot address are also used to address an input card slot. The remaining 12 bits are not relevant to the input cards. An input card's 12 data bit outputs are transmitted to the computer when an address word selects the associated input card slot and the multiprogrammer has been previously placed in the input mode.

1-25 When an input/output card is plugged into a particular slot of a particular unit, it assumes the address of that slot and unit, and will either receive and store data (output cards) or transmit data (input cards) only when that unit and slot are addressed. Unit selection is accomplished by decoding control words, as described previously, but slot address decoding is accomplished by directly wiring a unique combination of four slot address bits to each of the 15 input/output slots. If a card is moved to a new slot it assumes the address of that slot.

1-26 When one or more D/A voltage converter, D/A current converter, or voltage monitor cards are used in a 6940B (or a 6941B), and A6 voltage regulator card must be installed in slot 600 to supply operating power. This card contains four isolated +15 and −15 volt regulated supplies. One of the supplies has a 750mA capability while the remaining three can each provide up to 150mA.

1-27 All input/output cards are fabricated on a 4½" x 11" printed circuit card. The inner end of the card contains a dual 24 pin (48 pin total) printed circuit plug that can mate with any connector in slot 400 through 414. For analog-type output cards, the output quantity is taken from a terminal block located on the outer-end of the card; for digital-type input/output cards, the input/output bits are received/taken from a dual 15 pin printed circuit plug on the outer-end of the card. All external device wiring is routed through a false-bottom channel of the multiprogrammer unit to the user's system.

1-28 6941B Multiprogrammer Extender

1-29 Up to fifteen 6941B Multiprogrammer Extenders (U01 through U15) can be operated with a 6940B Multiprogrammer to extend the capacity of multiprogrammer systems to 240 input/output channels. The 6941B mainframe is physically similar to the 6940B, but has no provisions for local programming. The 6941B control panel contains only an ON/OFF power switch and associated indicator lamp.

1-30 The card cage, main dc power supply, adapter cards, and rear panel are the same for the 6941B as for the 6940B. However, the only mainframe plug-in cards required for operation of the 6941B are an extender unit input card A1, I/O transfer card A2, and logic and timing card A3. Slot 500, previously occupied by unit select card A5, is left blank. Slots 400 through 414 are still assigned to A4 input/output cards and slot 600 is reserved for a voltage regulator card.

1-31 The programmed data and address bits, 15 unit selection lines, and control and timing signals from the 6940B multiprogrammer are cabled to input jack J1 of the first 6941B extender unit in the system. Further, when the input mode is selected, extender unit input data is placed on the programmed data lines and on to connector J1 for application, along with control signals, to the 6940B Multiprogrammer.

1-32 When the input mode is not selected, the data and address bits are routed through input adapter card A7 to input card A1. After being properly terminated by card A1, the bits are selected and coupled through the A2 card in slot 200 to logic and timing card A3. When the input mode is selected, input data bits 0-11 from the A3 card are buffered on the A2 card and selected for output to the 6940B. Since the outputs of the A2 card selection logic are connected to the same lines as the output mode programmed data, the input

data is routed to connector J1 in place of programmed data for output to the 6940B.

1-33 The A3 logic and timing card in the 69418 extender unit is identical to the A3 card in the 69408 multiprogrammer. The A3 card selects either programmed data for application to the extender unit output card slots or it selects input card data for application to the A2 card and transmission back to the computer. The selection is based on the input mode control signal supplied to the 6941B from the 6940B. Like the 6940B A3 card, in addition, the 6941B A3 card generates a flag signal which is returned to the 6940B through the J1 connector and chaining cable, to indicate the busy-ready status of the 6941B extender unit Ø1.

1-34 The unit Ø1 select line of the 15 input unit select lines is wired to all input/output card slots of unit Ø1, while the remaining 14 unit select lines are jumpered directly from input jack J1 to output jack J2 after being buffered on the A8 output adapter card and then through a chaining cable to the next extender unit in the system. This process is repeated until at the 15th extender unit all unit select lines have been terminated at their associated unit.

1-35 When unit Ø1 is selected, its 400 through 414 input/output card slots are partially enabled. The next data or address word will enable one input/output card of unit Ø1 to receive programmed data (output) or transmit (input) data. The input/output data, unit select, and control and timing signals at output jack J2 are chain-cabled to input jack J1 of the next 69418 extender unit in the system.

1-36 ACCESSORIES

1-37 Tables 1-1 and 1-2, respectively, list the accessories furnished with and available for use with the 6940B. The descriptions of the available accessories in Table 1-2 are general and in no way represent complete specifications. Complete specifications are covered in the instruction manuals for each accessory.

Effective December 1, 1975, Rack Mounting Kit 5060-8741 is not longer a furnished accessory but it is still available as a standard option. The rack mounting kit is obtained by specifying Option 908 when ordering the instrument.

1-38 SPECIFICATIONS

1-39 Specifications for the 6940B Multiprogrammer are given in Table 1-3.

Table 1-1. Accessories Furnished

ACCESSORY	DESCRIPTION
Data Input Plug P1, Part No. 06936-60009	Mates with data input connector on 6940B; allows user to fabricate his own data input cable.
Rack Mounting Kit, Part No. 5060-8741	Allows 6940B to be rack mounted.
Plug-In Extender Card, Part No. 5060-7901	Extends plug-in cards out of the multiprogrammer chassis for trouble-shooting.

Table 1-2. Accessories Available

ACCESSORY	DESCRIPTION
MULTIPROGRAMMER EXTENDER, Model 6941B	Used with 6940B to increase the capacity of multiprogrammer systems. Each 6941B can accommodate up to 15 input/output cards. Up to fifteen 6941B's can be driven by one 6940B.
PROGRAMMABLE OUTPUT CARDS: Programmable Resistance Cards: Model 69500A	A versatile programmable output card that can be configured by the user to provide one 12-bit or two 6-bit output channels. Output resistors are not loaded on this model. The choice of output component value is left to the user.

Table 1-2. Accessories Available (Continued)

ACCESSORY	DESCRIPTION
Models 69501A through 69506A	Provides a single 12-bit resistance programming channel; the programming coefficients of these models are compatible with HP Programmable Power Supplies.
Models 69501A through 69513A	Provides two 6-bit resistance programming channels; these models are designed for programming the current limit of HP Programmable Power Supplies.
Bipolar Power Supply/Amplifier Control Cards, Models 69325A through 69328A.	Provide resistance outputs to control the voltage programming (69325A), current limit programming (69326A or 69327A), and gain programming (69328A) of HP Bipolar Power Supply/Amplifiers.
Relay Output Card, Model 69330A	Provides 12 separate form A (SPST, normally open) mercury-wetted contact outputs that reflect the status of 12 programmed data bits. Includes gate/flag circuits for exchange of control signals with user's device.
Relay Output/Readback Card, Model 69433A	Provides same outputs as Model 69330A; also supplies 12 input data lines that can be read by the computer and which indicate the relay coil voltage status.
D/A Voltage Converter Card, Model 69321B	Provides programmable voltage output from +10V to -10V at programming speeds of $<50\mu$sec.
D/A Current Converter Card, Model 69370A	Provides programmable current output from 0 to 20mA at programming speeds of $<100\mu$sec.
Voltage Regulator Card, Model 69351A	Required for use with D/A Voltage Converter, D/A Current Converter, and A/D Voltage Monitor cards. Installed in multiprogrammer slot 600 to provide ±15Vdc operating voltage for these cards.
Digital Output Card, Model 69331A	Provides programmed microcircuit logic level outputs on 12 separate output lines. Card includes gate/flag circuits for exchange of control signals with user's device.
Open Collector Output Card, Model 69332A	Provides 12 solid state output switches to control lamps and relay coils using an external dc power source. Each output circuit is rated at up to 30Vdc and 40mA.
Stepping Motor Card, Model 69335A	Provides 1 to 2047 pulses from either of two output terminals on receipt of one computer word. These pulses, when applied to the stepping motor translator, are converted to CW and CCW drive pulses for a stepping motor.
Breadboard Output Card, Model 69380A	Allows customer to design and build a custom analog or digital output card. Card includes basic address, storage, and control signal buffer circuits.
PROGRAMMABLE INPUT CARDS: Digital Input Card, Model 69431A	Accepts 12 bits of TTL, DTL, or contact closure data from user's device. Card includes gate/flag circuits for exchange of control signals with user's device. Outputs to computer reflect the status of 12 input bits.

Table 1-2. Accessories Available (Continued)

ACCESSORY	DESCRIPTION
Isolated Digital Input Card, Model 69430A	Accepts 12-bits of input data from user's device. All input lines are isolated from one another and from the multiprogrammer power supply. Eight options of the card are available to accommodate either ground-true or positive-true logic sense inputs and a wide range of input levels.
Event Sense Card, Model 69434A	Compares the magnitude of an external 12-bit input word with a stored reference word and generates a computer interrupt for any of four conditions, depending on the placement of a jumper on the card. The four possible conditions are: In=Ref, In≠Ref, In>Ref, In<Ref. The reference word is loaded from the computer. Both the input and reference words can be read back to the computer.
Voltage Monitor Card, Model 69421A	Monitors dc voltages in the range of +10.235V to −10.240V and returns a 12-bit binary word to the computer that indicates the magnitude and sign of the measured voltage. An optional version of the card has an input voltage range of +102.35V to −102.40V.
PROGRAMMABLE INPUT CARDS: Pulse Counter Card, Model 69435A	Counts pulses or contact closures, up or down, in the range of 0 to 4095. It can be preset by the computer to any value in this range and can have its contents read into the computer. When used in conjunction with a Programmable Timer Card or Frequency Reference Card, it can make frequency or time interval measurements.
Programmable Timer Card, Model 69600A	Generates a single crystal-controlled pulse each time it is commanded by the program. The duration of the pulse can be programmed in the range 1 to 4095 times a jumper-selectable interval that can have any of six decade values ranging from 1μsec to 0.1sec. When used to provide an enable to a Pulse Counter Card for frequency measurements, the 69600A may be armed to request a computer interrupt for the Pulse Counter Card at the end of the programmed time interval.
Frequency Reference Card, Model 69601A	Provides crystal-controlled squarewave outputs at fixed frequencies from 1 Hz to 100 kHz. The 69601A may be used in conjunction with the Pulse Counter Card for time interval measurements.
Breadboard Input Card, Model 69480A	Allows customer to design and build a custom input card. Card includes basic address and readback circuits.
Process Interrupt Card, Model 69436A	Generates an interrupt whenever any one of 12 inputs changes state (1 to 0, 0 to 1, or both). Bit(s) that changed state are readback by the controller.
CHAINING CABLE ASSEMBLY, Model 14541A	Interconnects 6940B and 6941B's in expanded Multiprogrammer Systems.
SERVICE AIDS: Pocket Programmer, Model 14533B	Permits manual programming of all input functions to the 6940B by switch closures. Plugs directly into data input connector J1 of 6940B.
Extender Cable for Pocket Programmer, Model 14534A	Affords additional convenience when using the Pocket Programmer by extending it 3-feet from the data input connector of the 6940B.

Table 1-2. Accessories Available (Continued)

ACCESSORY	DESCRIPTION
INTERFACING ACCESSORIES:	
HP Computer Interface Kit, Model 14550A Kit includes: a. Driver Tapes and Software Manuals b. Verification Kit, including 69431A (opt. 095) Input Card, 69331A Output Card, slot verification cable, and Diagnostic Tape. c. Microcircuit Interface I/O Card, Model 12566B (modified) d. Main Input Cable Assembly, Model 14540A.	Contains necessary hardware and software to interface HP Computers with 6940B Multiprogrammer, and verify system operation.
Main Input Cable Assembly, Model 14540A	Connects microcircuits interface I/O card, Model 12566B to 6940B Multiprogrammer (this cable is also part of Interface Kit, Model 14550A).

Table 1-3. Specifications

INPUT POWER:

100Vac (+5%, −10%), 48-440Hz, 4A
120Vac (+5%, −10%), 48-440Hz, 4A
220Vac (+5%, −10%), 48-440Hz, 2A
240Vac (+5%, −10%), 48-440Hz, 2A
} Selectable

DATA WORD TRANSFER RATE:

20K word/sec (maximum in handshake mode).

DATA RESOLUTION: 12 bits.

TEMPERATURE RANGE:

Operating: 0^{o} to $+55^{o}$C.
Storage: -40^{o} to $+75^{o}$C.

OPERATING POSITION:

30 degrees off horizontal (maximum).

DIMENSIONS: See Figure 2-1.

COOLING: Natural convection.

1-40 COMPUTER INTERFACING

1-41 All 6940B Multiprogrammers are supplied with a standard A1 input card. This card provides the proper termination for the driver circuits of digital programming sources employing TTL or DTL microcircuit logic. The input data must also have ground-true logic levels (logical 1 = LO; logical 0 = HI). Voltage and current requirements for the digital source driver circuits are given in Section III.

1-42 Return data bits 0-11 and 15 to the computer from the multiprogrammer are produced by drivers which can supply either TTL or DTL microcircuit logic levels or higher voltage logic levels at the option of the user. The returned flag signal, however, is supplied only at the microcircuit logic level. In addition, the output data and flag have ground-true logic sense. If other logic sense or voltage levels are required, they must be interfaced at the user's programming device.

1-43 As supplied from the factory, the 6940B is configured for operation from a 120Vac (+5%, −10%), 48-440Hz power source. The 6940B can also be operated from a 100, 220, or 240Vac (+5%, −10%), 48-440Hz power source by changing the position of the PC board (voltage selection board) within the ac power module on the rear panel. (See paragraph 2-23). Ensure that the proper line fuse (F1) (4A for 100V/120V or 2A for 220V/240V) is installed. Also, ensure that the proper fuse values for F2 (10A) and F3 (.75A) are installed. F2 and F3 are located on the rear panel.

1-44 INSTRUMENT IDENTIFICATION

1-45 Hewlett-Packard instruments are identified by a three-part serial number. The first part is the instrument model number. The second part is the serial number prefix, consisting of a number-letter combination denoting the date of a significant design change. The first two digits indicate the year (10 = 1970, 11 = 1971, etc.); the second two digits indicate the week; and the letter "A" designates the U.S.A. as the country of manufacture. The third part is the instrument serial number; a different 5-digit sequential number is assigned to each instrument, starting with 00101.

1-46 If the serial number on your instrument does not agree with those on the title page of this manual, Change Sheets supplied with the manual define the differences between your instrument and the instrument described by this manual.

1-47 OPTION 001

1-48 Option 001 modifies the 6940B and 6941B so that they are compatible with 6940A/6941A multiprogrammer systems and software. Since 6940A's and 6941A's have been discontinued, Option 001 must be specified by customers ordering a replacement 6940B or additional 6941B's for use in a 6940A/6941A multiprogrammer system. Appendix A in the rear of this manual describes the 6940B Option 001 modifications. The 6941B Option 001 modifications are described in the 6941B instruction manual.

1-49 ORDERING ADDITIONAL MANUALS

1-50 One manual is shipped with each instrument. Additional manuals may be purchased from your local Hewlett-Packard field office (see list at rear of this manual for addresses). Specify the model number, serial number prefix, and HP Part number shown on the title page.

1-51 Effective December 1, 1975, extra manuals may be obtained by specifying Option 910 when ordering your instrument. The number of extra manuals depends upon the number of Option 910's ordered.

SECTION II
INSTALLATION

2-1 INITIAL INSPECTION

2-2 Before shipment, this instrument was inspected and found to be free of mechanical and electrical defects. As soon as the instrument is received, proceed as instructed in the following paragraphs.

2-3 Mechanical Check

2-4 If external damage to the shipping carton is evident, ask the carrier's agent to be present when the instrument is unpacked. Check the instrument for external damage such as broken controls or connectors, and dents or scratches on the panel surfaces. If the instrument is damaged, file a claim with the carrier's agent and notify your local Hewlett-Packard Sales and Service Office as soon as possible (see list at rear of this manual for addresses).

2-5 Electrical Check

2-6 Check the electrical performance of the instrument as soon as possible after receipt. Section V of this manual contains checkout procedures which will verify instrument operation. Refer to the inside front cover of the manual for the Certification and Warranty statements.

2-7 REPACKAGING FOR SHIPMENT

2-8 To insure safe shipment of the instrument, it is recommended that the package designed for the instrument be used. The original packaging material is reusable. If it is not available, contact your local Hewlett-Packard field office to obtain the materials. This office will also furnish the address of the nearest service office to which the instrument can be shipped. Be sure to attach a tag to the instrument specifying the owner, model number, full serial number, and service required, or a brief description of the trouble.

2-9 INSTALLATION DATA

2-10 The 6940B is shipped with all standard main frame cards (A1, A2, A3, and A5) installed. To prepare the 6940B for operation in a system, it is necessary to rack-mount it and any 6941B's, install the required accessory (input and output) cards, and connect signal and power cables.

CAUTION

Always turn off power to the multiprogrammer before removing or installing printed circuit cards (standard mainframe cards or accessory cards). If power is not removed, it is possible to cause damage by shorting components.

2-11 Location

2-12 The 6940B and 6941B are convection cooled. When mounted in a rack, a minimum of 0.25 inch (and preferably 1 inch) should be left between units so that a free flow of cooling air can reach internal components. The units should be installed in an area where the ambient temperature remains between 0°C and +55°C.

2-13 Outline Diagram

2-14 Figure 2-1 illustrates the outline shape and dimensions of the 6940B.

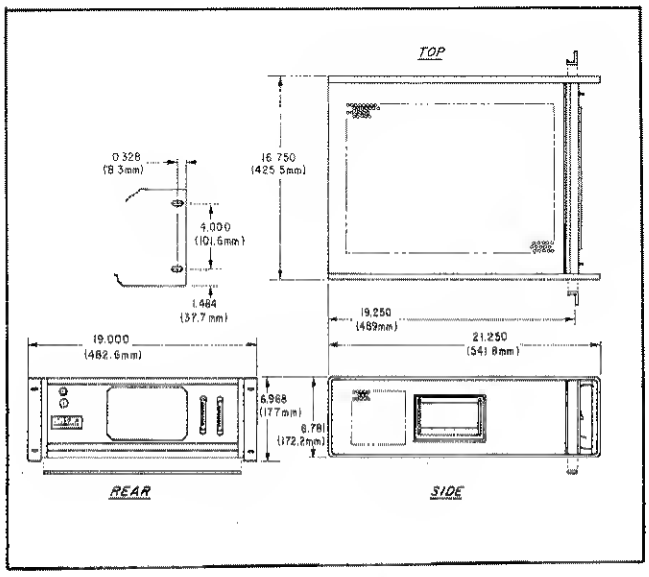


Figure 2-1. Outline Diagram

2-15 Rack Mounting

2-16 An instruction card attached to the 6940B rack mount-

ing kit (supplied with each unit) illustrates and describes the procedure for preparing the 6940B for rack mounting.

2-17 Accessory Card Installation

2-18 Before installing accessory cards, be sure to first perform the 6940B checkout procedure given in Section V of this instruction manual. Accessory cards are installed in slots 400 through 414. To install the cards, proceed as follows:

a. Open the hinged front panel of the unit by turning the recessed screw within the knurled handle counterclockwise.

b. With the accessory card components on the right, slide the card into the desired slot (400 through 414). Note that all accessory cards are slotted between pins 4 and 5 and all 400 series connectors on the main frame are keyed between the same points. This makes it virtually impossible to plug an accessory card in upside down or into any other than a 400 series slot.

c. Route all wiring from the accessory cards through the false-bottom channel and out the back of the unit to the external system. Special wiring considerations are covered in the instruction manuals for the individual accessory cards.

d. As installation is completed for each accessory card, carefully note and record the following types of information on the installation record card located on the rear of the hinged front panel.

(1) Accessory card type
(2) Application in external system
(3) Nature of input or output signals
(4) Ranges, scaling factors, polarity, logic sense, etc.

2-19 System Cabling

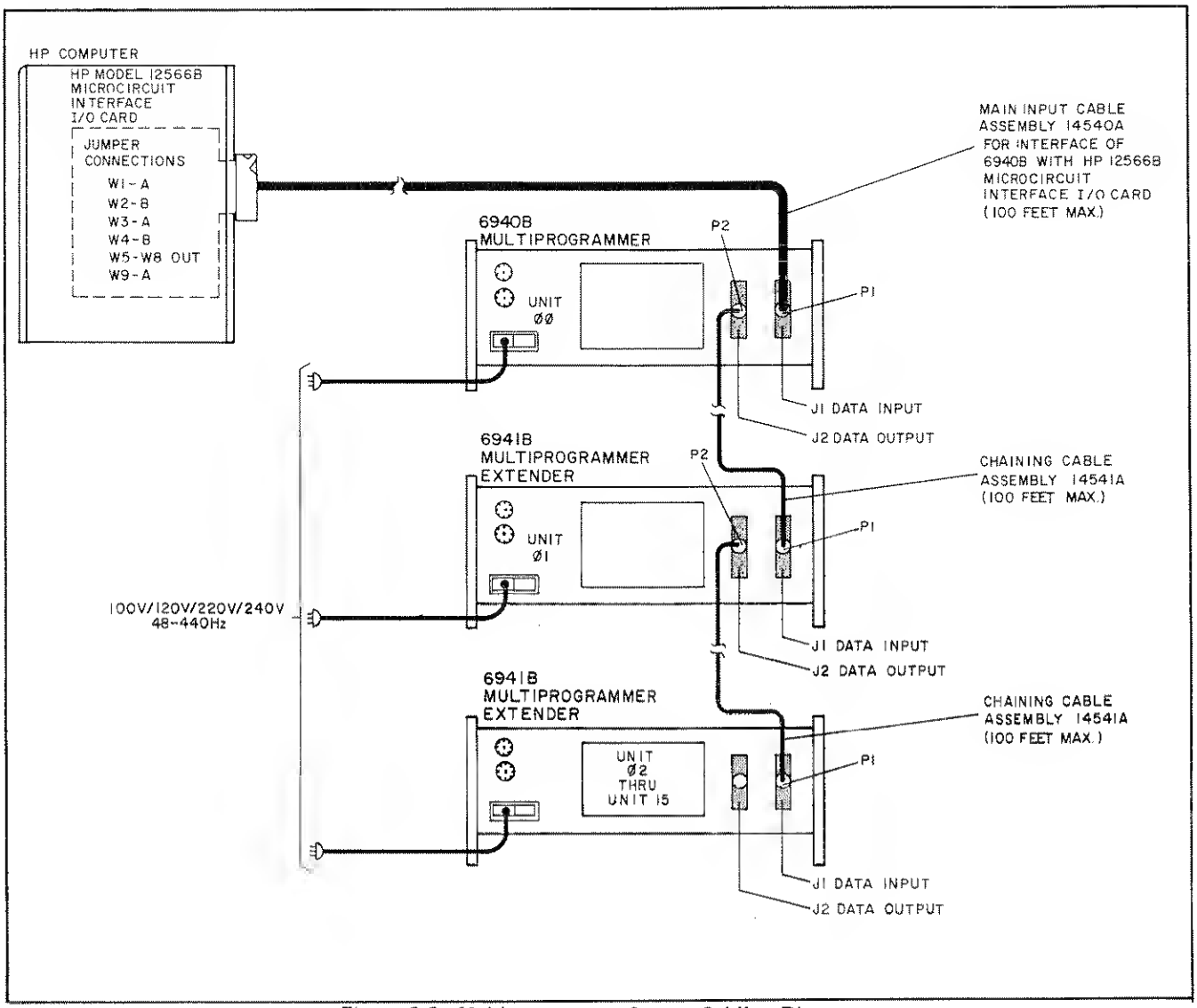


Figure 2-2. Multiprogrammer System Cabling Diagram

2-20 The 6940B/6941B Multiprogrammer System is designed to operate with distances of up to 100 feet between units. Because of this design, programmed delays are required in the 6940B/6941B system software (see paragraph 3-133). Thus, 6940B/6941B units are not compatible with the discontinued 6940A/6941A units. Consequently, B units and A units may not be mixed in a multiprogrammer system. Option 001, however, is available (see paragraph 1-49) which converts the 6940B/6941B units to operate in a 6940A/6941A system. This option allows a customer to purchase replacement or additional units for an existing 6940A/6941A system.

2-21 A system cabling diagram is given in Figure 2-2. This diagram shows an HP computer using a type 12566B Microcircuit Interface I/O card as the programming source, and cable assembly 14540A connecting the I/O card to the 6940B. The jumper connections shown on the Microcircuit Interface card establish the proper computer gate-multiprogrammer flag logic sense relationships and allow the computer to perform a monitor data check without the need for the multiprogrammer system flag to return from the "busy" to the "ready" state. (See the Instruction Manual for the 12566B Microcircuit Interface I/O Card for additional details). Cables of various lengths up to 100 feet maximum, can be purchased from your local Hewlett-Packard field office (see list at rear of this manual for addresses). The 14540A Main Input Cable Assembly can be ordered specifying any length from 12 feet to 100 feet maximum. Data plug P1 is supplied with all 6940B's to enable the user to fabricate his own data input cable, as required.

2-22 Step-by-step cabling procedures are given as follows:

a. Connect data input plug P1 to DATA INPUT connector J1 on the rear of the 6940B.

NOTE

A jumper on data input plug P1 (pin 18 to pin 19) completes the system enable circuit within the 6940B. Plug P1, therefore, must be in place before the multiprogrammer system can be enabled.

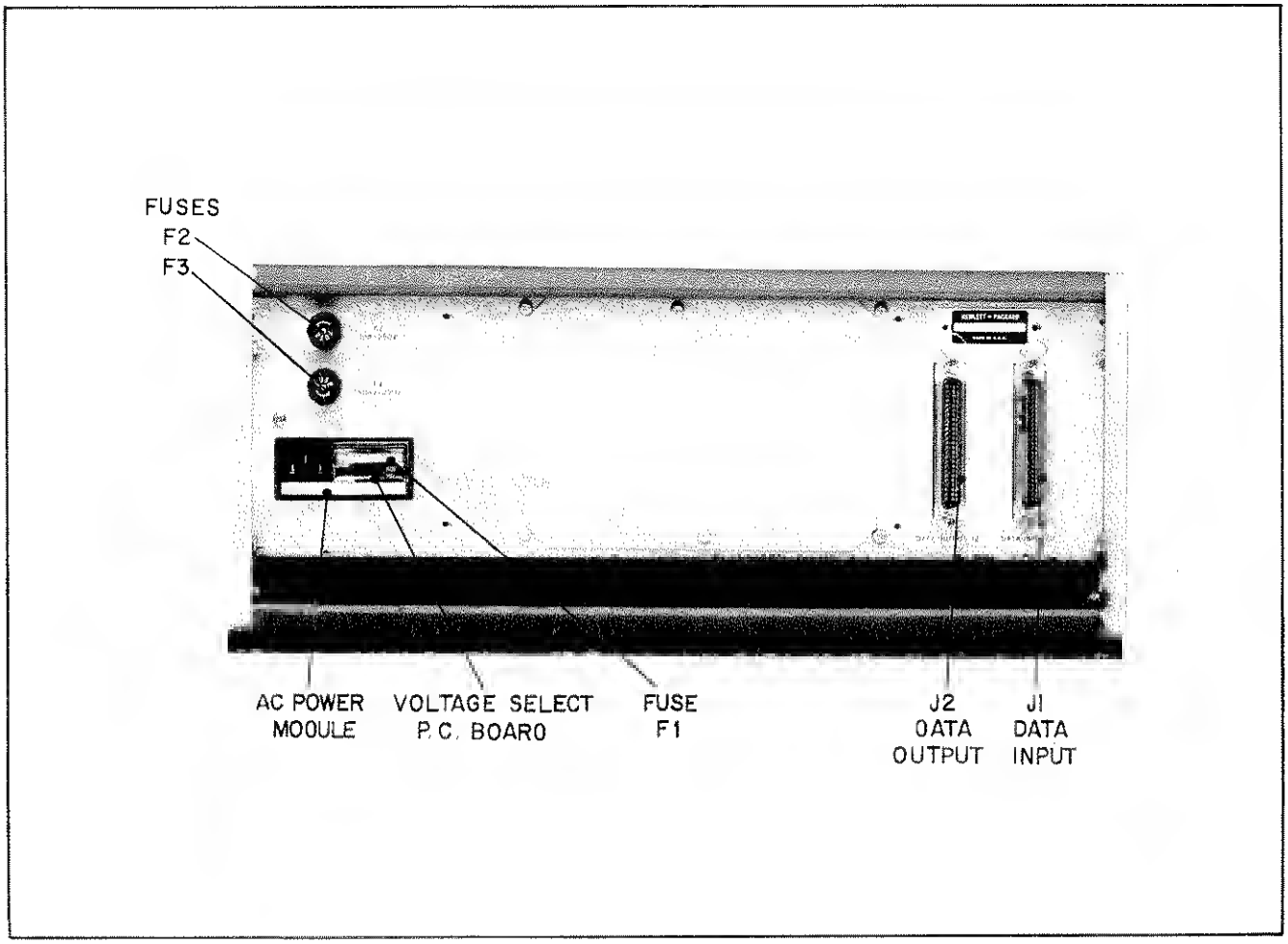


Figure 2-3. 6940B Multiprogrammer, Rear View

b. Using chaining cable assembly 14541A, connect DATA OUTPUT connector J2 on the 6940B (unit ØØ) to DATA INPUT connector J1 on the first 6941B extender unit (unit Ø1) in the system. (If no extender units are used, DATA OUTPUT connector J2 on the 6940B is left open.)

c. Continue chain-cabling the J2 DATA OUTPUT connector of each extender unit to the J1 DATA INPUT connector of the next higher-numbered extender unit in the system.

d. Before connecting power to the units, refer to the following paragraph and Section III.

2-23 INPUT POWER REQUIREMENTS

CAUTION

Failure to correctly match the Multiprogrammer's primary voltage setting to the available source may result in damage to the instrument.

2-24 The 6940B and 6941B may be operated continuously from a nominal 100V, 120V, 220V, or 240V (48-440Hz) power source. A printed circuit board located within the ac power module on the rear panel (Figure 2-3) selects the power source. Voltage choices are available on both sides of the PC board. Before connecting the instrument to the power source, check that the PC board selection matches the nominal line voltage of the source. The operating voltage is shown in the window of the ac power module (Figure 2-4). If required, select the proper voltage as follows (refer to Figure 2-4):

a. Remove power cable from instrument.

b. Move plastic door on power module aside.

c. Rotate FUSE PULL to the left and remove line fuse F1.

d. Remove PC board from slot. Select operating voltage by orienting PC board to position the desired voltage on top-left side of PC board. Push board firmly into slot.

e. Rotate FUSE PULL back into normal position and re-insert fuse F1 in holder using caution to select the correct value for F1 (4A for 100V or 120V and 2A for 220V or 240V).

f. Close plastic door and connect power cable.

2-25 When the instrument leaves the factory, the proper fuse is installed for 120V operation. An envelope containing a fuse (2A) for 220V/240V operation is attached to the instrument. Make sure that the correct fuse value for F1 is installed if the position of the PC board is changed.

2-26 Also, before connecting the instrument to the power source, ensure that the proper fuse value is installed for F2 (10A) and F3 (.75A). Fuses F2 and F3 are located on the rear panel as shown in Figure 2-3. Fuse F2 is in the +5V (reg)/+12V (unreg.) circuit and F3 is in the −12V (unreg.) circuit of the main power supply.

2-27 Power Cable

2-28 To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the instrument panel and cabinet be grounded. This instrument is equipped with a three conductor power cable. The third conductor is the ground conductor and when the cable is plugged into an appropriate receptacle, the instrument is grounded. The offset pin on the power cable's three-prong connector is the ground connection.

2-29 To preserve the protection feature when operating the instrument from a two-contact outlet, use a three-prong to two-prong adapter and connect the green lead on the adapter to ground.

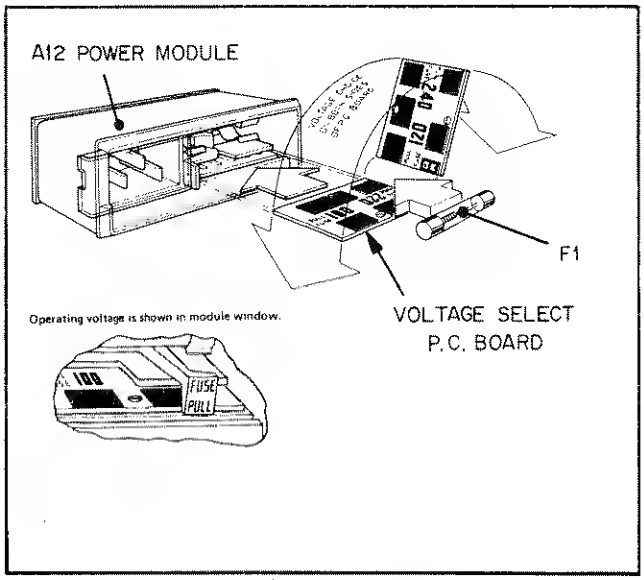


Figure 2-4. Line Voltage Selection

SECTION III
OPERATING INSTRUCTIONS

3-1 PRE-OPERATIONAL CONSIDERATIONS

WARNING

Turn off all external power supplies associated with this unit before servicing it or changing any external connections. High voltages may be present on printed circuit boards even when ac power is removed from the unit.

CAUTION

Remove ac power before inserting or removing I/O cards.

3-2 Before applying power to the unit, ensure that the proper operating voltage (100V, 120V, 220V, or 240V) has been selected as described in paragraph 2-23. All system cable connections (Between the computer and the 6940B Multiprogrammer and between the 6940B and any 6941B Multiprogrammer Extenders that may be employed) should be made as outlined in Section II of this manual.

3-3 **Input/Output Cards.** Input/Output cards should be inserted into the desired slots (400 through 414) of the 6940B card cage. All input/output cards are marked as to type on the card extractor handles. Notice that whenever a programmable input/output card is inserted into a slot (400 through 414) it assumes the address of that particular slot position. The method of addressing a particular card slot is described later in this section, under Remote Programming. Detailed information about each input/output card is contained in the instruction manual associated with each card.

3-4 **Pre-Operation Checkout.** Before connecting system loads to any of the input/output cards, perform the basic checkout procedures given in Section V of this instruction manual.

3-5 If the checkout procedure results are satisfactory, external device connections can be made to the cards (as described in the card manuals) and the unit operated normally.

3-6 INTERFACING

3-7 All data and control information that is exchanged between the 6940B and the computer (or other external control source) passes through data input connector J1 on the rear panel (see Figure 3-1). The 16 computer data bits as well as the computer gate and multiprogrammer flag signals are all interfaced on multiprogrammer input card A1 (located in slot 100). The 13 return data bits are sent from the 6940B to the computer from either the 6940B A3 Logic and Timing card (located in slot 300) or the 6940B A2 Remote/Local card (located in slot 200). The A3 card interfaces bits 0-11 while the A2 card interfaces bit 15. (Bits $\overline{B12}$, $\overline{B13}$, and $\overline{B14}$ are not connected for return to the computer.) The following paragraphs describe the input card and the return data interface driver circuits located on the A3 and A2 cards. These descriptions are followed by a brief discussion of the data parameters associated with each of the input/output lines listed on Figure 3-1.

3-8 Standard Input Card

3-9 The standard input card interfaces with binary programming sources employing microcircuit logic of the TTL or DTL family. It was designed specifically for use with a Hewlett-Packard computer employing a 12566 Microcircuit

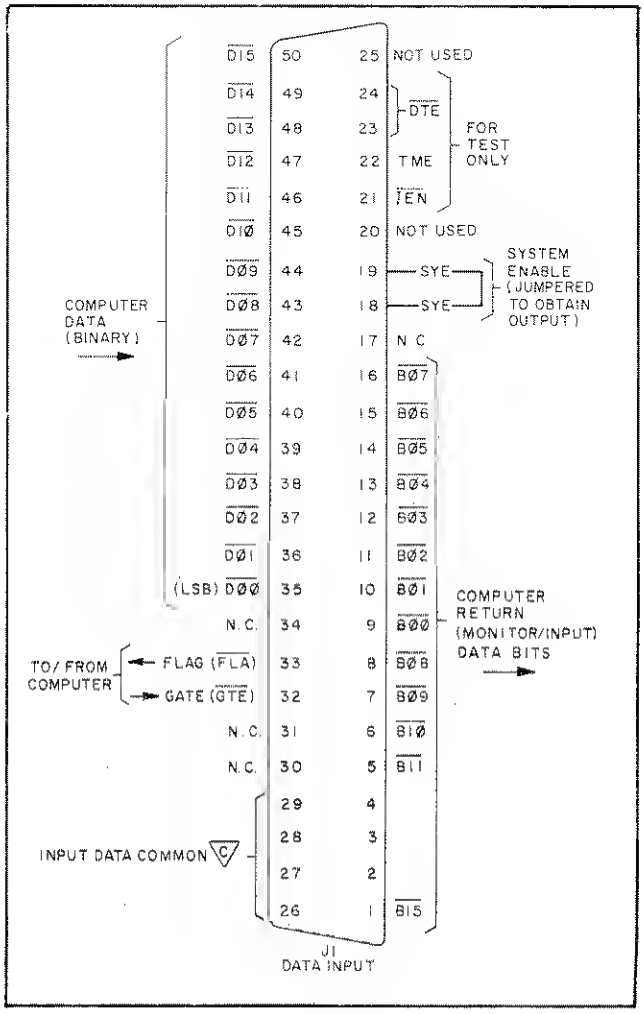


Figure 3-1. Data Input Connector

Interface Input/Output card. One 12566 I/O card can accommodate up to 16 multiprogrammer units; i.e., one complete multiprogrammer system consisting of one 6940B and fifteen 6941B extender units.

3-10 **Receiver Circuit.** Figure 3-2 shows a typical receiver circuit that is used for each of the 16 data bits and the gate input. Also shown on the drawing are the basic specifications of each receiver circuit. The maximum current that is sourced (delivered) by a receiver circuit if the input terminals are shorted is 19mA. The maximum current that can be sinked (absorbed) by a receiver circuit with a +5.5V input is 2.6mA. E_{OC} is the nominal voltage across the input terminals when they are open circuited.

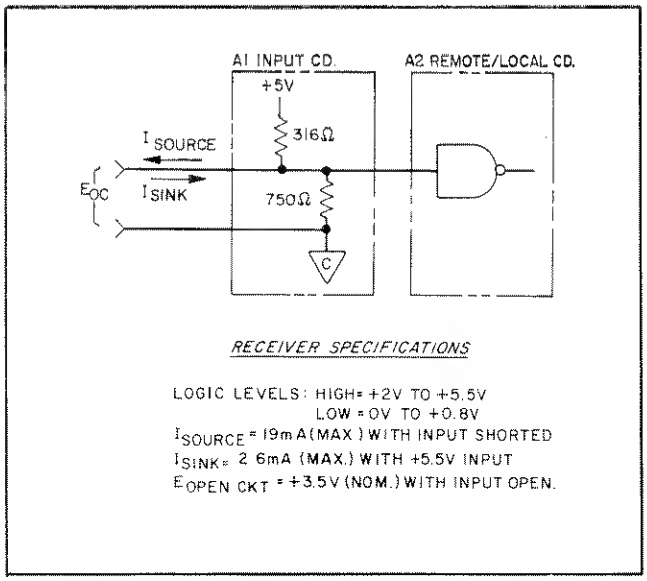


Figure 3-2. Typical Receiver Circuit, Standard Input Card

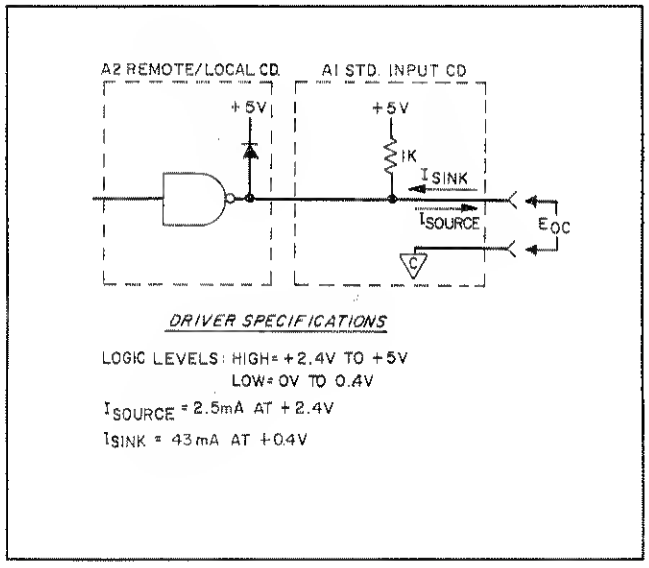


Figure 3-3. Flag Driver Circuit, Standard Input Card

3-11 **Flag Driver Circuit.** Figure 3-3 shows the driver circuit that is used for the multiprogrammer flag output line. The circuit consists of a driver stage and diode clamp on the A2 board and a 1k pullup resistor returned to +5V on the A1 board.

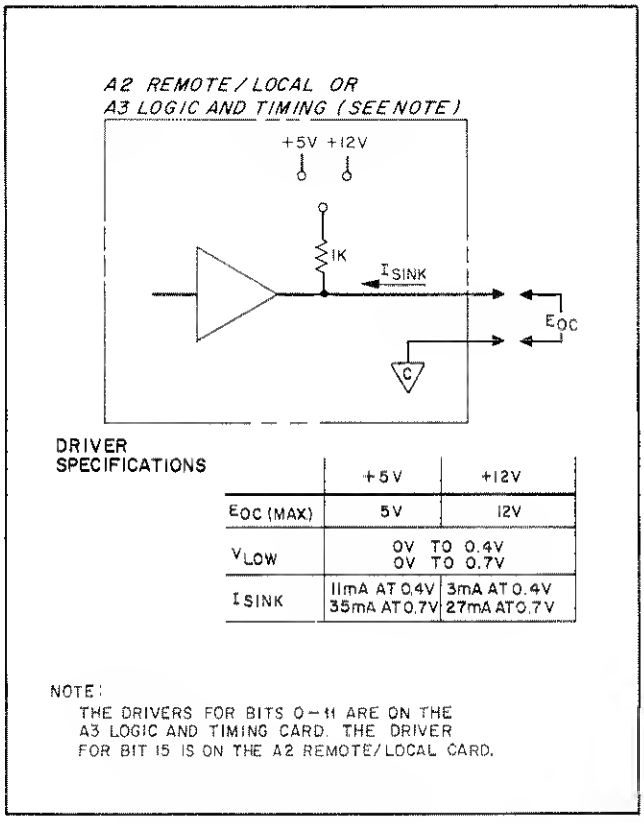
3-12 Return Data Driver Circuit

3-13 Figure 3-4 shows the driver circuit that is used for the 13 return data bits. The return data bits do not pass through the A1 input card. Bits 0-11 are sent from the A3 Logic and Timing Board and bit 15 is sent from the A2 Remote/Local Board. The output circuits for all return data drivers, however, are identical and provide a 1k pullup resistor returned to either +5V or +12V at the option of the user.

3-14 Computer Data Bits

3-15 The 16 parallel computer data bits ($\overline{D00}$ through $\overline{D15}$ must be received in binary form. The data bits can be received in one of three word formats; control word, address word, or data word, as will be explained under remote programming later in this section.

3-16 **Logic Coding.** For interfacing with the standard input card, the data must be received in negative-logic form



	+5V	+12V
E_{OC} (MAX)	5V	12V
V_{LOW}	0V TO 0.4V 0V TO 0.7V	
I_{SINK}	11mA AT 0.4V 35mA AT 0.7V	3mA AT 0.4V 27mA AT 0.7V

Figure 3-4. Typical Driver Circuit, Return Data Bits

(ground-true, positive-false). This means simply that a programmed binary 1 = LO and a binary 0 = HI. Notice, however, that the internal logic circuits of the 6940B have been designed within a framework of positive logic (binary 1 = HI, binary 0 = LO). Hence, the 6940B employs a positive-logic system with complemented (negative true) inputs (see Section IV for a detailed definition).

3-17 Computer Gate Input

3-18 The computer gate (or encode) input is an action command that is sent to the internal timing circuits of the 6940B to initiate data storage and/or processing functions within the 6940B at the discretion of the computer. To control the mode of operation of the 6940B, for instance, the computer must transmit a mode control word which is stored (and subsequently processed) in the 6940B when it also receives the computer gate. Similarly, in order to output data (write) to a multiprogrammer output card, the computer must accompany the data word with the computer gate. When it receives the computer gate, the multiprogrammer timing circuits initiate storage of the data in the addressed output card. Input data reception (read) by the computer from a multiprogrammer input card, on the other hand, does not require the computer gate. The computer need only address an input card in the correct mode and the card data is transferred from the input card to the computer. However, the computer must send the computer gate in order to activate input cards. When activated, the input card's gate-flag interface with the external device is initiated which ultimately (when the device flag input to the input card goes ready) results in the storage of input data on the input card. In addition, when activated, the input card interrupt capability is enabled which, if the associated mode of operation has been established, allows the input card to control the multiprogrammer's flag line to the computer and, thus, provides a means for the card to signal the computer that data is ready. To activate an input card, the computer gate must be received in the correct mode by the multiprogrammer timing circuits which initiate the activation of the addressed input card. Upon activation, the input card, in turn, initiates a data input cycle with its associated external device. Similarly, an input card is de-activated (which means, essentially, that its interrupt capability is turned off), when the card is addressed in the correct mode and the computer gate is received.

3-19 A HI to LO transition of the computer gate initiates the required action (see Figures 3-11 and 3-12). Further information regarding the gate input and other timing functions is provided in the discussions of the output and input data modes of operation provided in Paragraphs 3-62 and 3-74.

3-20 6940B Flag Output

3-21 The flag output of the 6940B is a response line to the computer the meaning of which depends upon the mode of operation established by the computer. The flag line is used to indicate busy-ready status of the multiprogrammer.

3-22 For data output modes of operation, when the 6940B flag output is in the ready state, input data can be applied to the multiprogrammer. When the flag switches to the busy state, computer data is being stored and processed in the 6940B and new data cannot be sent until the flag line again goes to the ready state. Two types of flags can be issued, handshake and timing, as described in Paragraph 3-109.

3-23 For data input modes of operation, the flag line also indicates that the multiprogrammer is ready with data for the computer or that it is busy and waiting for data input from an external device. Like output data transfers, two types of flags are utilized (the handshake and timing) during input modes but their usage depends on the type of input data transfer desired. That is, the handshake and timing flags have different meanings if data inputs involve one input card or many input cards. Paragraph 3-114 describes typical methods by which the computer uses the flag to interface with the 6940B input cards. For the standard interface configuration, the flag is HI (+2.4V to +5V) when ready or LO (0V to +0.4V) when busy.

3-24 $\overline{\text{ISL}}$, $\overline{\text{DTE}}$, TME, $\overline{\text{IEN}}$, and $\overline{\text{IRQ}}$

3-25 $\overline{\text{ISL}}$, $\overline{\text{DTE}}$, TME, and $\overline{\text{IEN}}$ are mode signals derived from programmed control words. The mode control signals are stored in the 6940B and distributed through data output connector J2 to all 6941B's in the system. The $\overline{\text{DTE}}$, TME, and $\overline{\text{IEN}}$ signals are brought to data input connector J1 for test purposes only. Similarly, input card request identification control signal $\overline{\text{IRQ}}$ (which is a common signal line for all input cards) is distributed to the 6941's through connector J2. When the pocket programmer is used for testing, the signals can be monitored at appropriate test jacks.

3-26 System Enable Interlock Jumper

3-27 A connection is made between pins 1B and 19 of the data input connector through the input plug. If this connection is removed, or if the input plug is removed, all output cards in the multiprogrammer system are disabled. The state of the internal SYE line is determined by bit DØ5 of an input control word (refer to Paragraph 3-64).

3-28 Return Data Bits

3-29 For output (write) modes of operation (ISL bit 7 = 0), bits $\overline{\text{BØØ}}$ through $\overline{\text{B11}}$ and $\overline{\text{B15}}$ are a reflection of the data bits received from the computer and may be used by the computer to monitor the data it sent in order to verify interface connections to the multiprogrammer. This procedure is often referred to as "echo" checking.

3-30 For input (read) modes of operation, when the input select (ISL) mode has been programmed, bits 0-11 of the return data lines carry the corresponding bits of the addressed input card. In addition, the multiprogrammer common input card input request (IRQ) line is combined with bit 15 within the multiprogrammer and returned to the computer on the return data bit 15 line. Bits 12, 13, and 14 are not connected for return to the computer.

3-31 The return data bits (0-11 and 15) are also returned to the computer during output mode (ISL off) local programming and reflect the status of the bit switches on the front panel. For input mode local programming (ISL on), return data bits 0-11 still carry the input card data (these bit switches are disabled) while bits 12-15 reflect the bit switches on the front panel. The input request identification line, IRQ, is displayed with the RETURN DATA lamp (see below).

3-32 Multiprogrammer—External Device Interfacing

3-33 The multiprogrammer input/output cards interface user devices (one device/card) with the computer via the multiprogrammer mainframe circuits. A wide variety of multiprogrammer input/output cards are available to satisfy many different user requirements. While the individual input/output card instruction manuals define the specific interface requirements, the following paragraphs describe the general interface capabilities provided by the input/output cards.

3-34 **Output Cards.** Multiprogrammer output cards process computer data (up to 12 bits) for interface with the associated external device. Output cards are available to: (1) interface digital data (the 12-bit computer data is transferred to the user's device); (2) convert the data to a specified analog voltage; (3) convert the data to a resistive value for remote programming of power supplies; (4) convert the data to a specified current; or (5) convert the digital data to equivalent relay contact closures. The output cards contain either timing circuits that can be set to synchronize the data transfers from the computer to the user's device (assuming the timing mode is programmed; i.e., TME bit 4 = 1) or timing circuits that exchange control signals with the external device to synchronize data output operations.

3-35 **Input Cards.** Multiprogrammer input cards process 12-bit user data for application to the computer. Input cards are available to (1) input 12-bit digital data (with voltage polarity and logic sense options provided), or (2) convert 12-bit relay contact closure data to digital data for input to the computer. Depending on the model selected, the input cards are also available with input card gate/user device flag timing circuits that allow the computer to be synchronized with the user's device through the input card. The requirements for the gate/flag signals are flexible and allow a variety of voltage polarity and logic sense specifications to be interfaced. Generally, however, the following gate/flag specifications should be met by the user's device when employing input cards with gate/flag timing circuit capabilities.

a. *Input Card Gate.* The leading edge of the input card gate indicates that the card can accept input data. The gate can be reset when the device flag goes busy or ready.

b. *Device Flag.* The device flag leading edge indicates to the input card that the device is busy processing data. At some time after the input card gate leading edge, the device flag should switch to the busy state. When the device has data for the computer, the device flag should be switched to the ready state (trailing edge). The ready transition of the device flag will cause the input card to notify the computer that data is ready. The device data must be available at the trailing edge of the flag and should be present for at least 10μsec (some input cards require a longer time period).

3-36 Input cards of the type described above (i.e., the digital data input card) are also available without gate/flag timing circuits. Data reception from these cards is completely controlled by the computer which must determine when data is ready from the associated external device. On the other hand, these cards provide for a maximum rate of data exchange from a user's device to the computer.

3-37 6940B — 6941B Interface

3-38 Unit select bits (UØ1 through U15), mode control signals ($\overline{\text{DTE}}$, TME, SYE, $\overline{\text{ISL}}$, and $\overline{\text{IEN}}$), and gate signal $\overline{\text{GAT}}$ are transmitted to the first 6941B in the Multiprogrammer System through multiprogrammer data connector J2 on the rear panel of the 6940B (see Figure 3-5). The Flag override ($\overline{\text{FOR}}$) and input request ($\overline{\text{IRQ}}$) signals are returned to the 6940B through J2, from the first 6941B in the system. Further, input/output data bits ($\overline{\text{B11}}$ through $\overline{\text{BØØ}}$) are exchanged between the 6940B and 6941B with the direction of data flow depending on the mode of operation. For output data transfers, all output data and address bits are transmitted to the first 6941B through connector J2. For input data transfers, bits $\overline{\text{B11}}$ through $\overline{\text{BØØ}}$ are returned from the 6941B to the 6940B through connector J2 and address bits $\overline{\text{B15}}$ through $\overline{\text{B12}}$, are transmitted to the 6941B by the 6940B. The functions of the above signals are described in the following paragraphs.

3-39 Unit Select Bits

3-40 Unit select bits UØ1 through U15 are transmitted to the extender units in positive-logic form (e.g., logic 1 = HI; logic 0 = LO). When the unit select card in the 6940B detects a control word, it decodes and stores the unit address bits that are programmed as part of the control word. The

unit select line associated with the selected unit will go HI and enable all input/output card slots of the selected unit. When a new unit is addressed, its associated U—— line will go HI and the previous unit select line will go LO (only one unit can be selected at a time). Subsequent data (output) or address (input) words will address and select one input/output card of the selected unit to receive (output) or transmit (input) data.

3-41 Mode Selection Bits SYE, TME, $\overline{DTE}$, $\overline{ISL}$, and $\overline{IEN}$

3-42 These bits are derived from programmed control words and transmitted to the extender units. The signals serve various control functions with each mode described in detail in Paragraph 3-58.

3-43 Gate Signal $\overline{GAT}$

3-44 Gate signal $\overline{GAT}$ is transmitted to all extender units to initiate actions on the input/output cards. For output cards, $\overline{GAT}$ initiates (when the card is also addressed) the storage of programmed data bits $\overline{B11}$ through $\overline{B\emptyset\emptyset}$. For input cards, $\overline{GAT}$ initiates (when the card is addressed) the gate/flag circuits on the input card or initiates the resetting of control circuits on the card depending upon the state of mode signal ISL. A HI to LO transition of $\overline{GAT}$ initiates these actions. Refer to Paragraphs 3-109 and 3-114 for additional details.

3-45 Flag Override ($\overline{FOR}$)

3-46 This signal is received by the 6940B from the first 6941B in the system and represents the busy-ready status of the input/output cards in the down-stream extender units. $\overline{FOR}$ controls the status of the $\overline{FLA}$ line returned to the computer by the 6940B.

3-47 Input/Output Data and Address Bits

3-48 Bits $\overline{B15}$ through $\overline{B\emptyset\emptyset}$ are exchanged between the 6940B and 6941B in ground-true form (e.g., logic 1 = $\overline{B15}$, LO; logic 0 = $\overline{B15}$, HI). The four most significant bits ($\overline{B15}$ through $\overline{B12}$) represent input/output card slot addresses and are always transmitted from the 6940B to the 6941B. Bits $\overline{B11}$ through $\overline{B\emptyset\emptyset}$, however, represent either data word output data (in which case they are transmitted from the 6940B to the 6941B) or input data from an addressed input card (in which case they are received by the 6940B from the 6941B). Notice that only output data words or input address words are meaningful in the extender units. The control word code (slot address 1111) serves no function in this case since extender units do not have a unit select card (and, of course, there is no input/output card slot number 16).

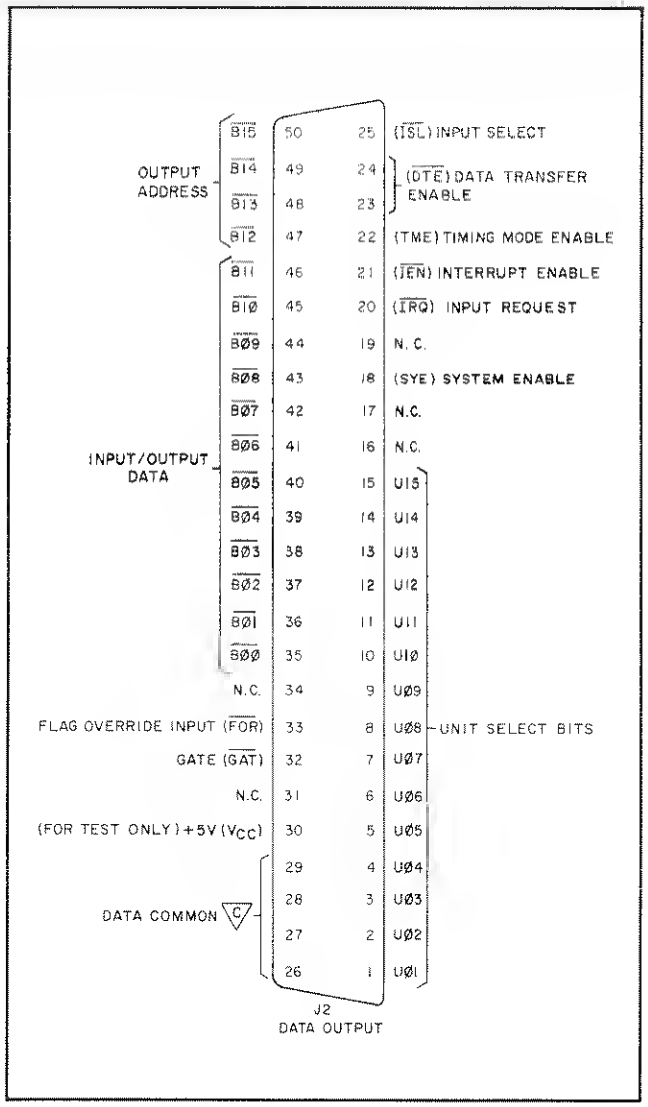


Figure 3-5. Data Output Connector

3-49 REMOTE PROGRAMMING

3-50 Remote programming is automatically selected when the LINE switch is first turned on. (Subsequently, programming can be switched between local and remote by pressing the front panel REMOTE/LOCAL switch). In remote, the multiprogrammer can be computer-programmed either to output data to an external device (through associated multiprogrammer output cards) or to input data from an external device (again, through associated input cards). Note that some multiprogrammer cards have a bidirectional capability. The Relay Output/Readback card, for instance, receives computer data (from the multiprogrammer mainframe circuits) during output data transfer modes while it returns the data (after processing) to the computer during input data transfer modes. Most multiprogrammer input/output cards, however, interface the computer/multiprogrammer mainframe with an associated external device in only one direction. Also, while the output and input data transfer modes may use separate, unrelated multiprogrammer cards, the modes are time-shared in the multiprogrammer mainframe. In addition, because

the multiprogrammer system is designed to operate with distance up to 100 feet between units, delays are required in the program when transferring data between the computer and the multiprogrammer system (See paragraph 3-133).

3-51 Multiprogrammer modes of operation are specified by 16-bit control words received (along with a computer gate signal) from the computer. The control words are identified by address bits 15-12 (see Figure 3-6) which, when they are all ones, specify the word as a mode control word. Note that when address bits 15-12 are any other configuration (0000-1110), the computer word is either a data word (output modes) or an address word (input modes).

3-52 In the output modes (previously specified, of course, by suitably-encoded control words), data words (and a gate signal for each word) are received from the computer for output to the addressed (bits 12-15 of the data word) output card. A programmed delay of 8μsec is required between data output to the multiprogrammer and setting the gate (see paragraph 3-133). Data words are transmitted to the multiprogrammer in one of two timing modes: the handshake mode or the timing (wait) mode. In the handshake mode, a computer data word is gated to the multiprogrammer which automatically responds after approximately 50μsec with a data ready flag back to the computer. Thus, data is transmitted by the computer without synchronization with the output card (or its external device). In the timing mode, on the other hand, a computer data word is gated to the multiprogrammer which waits until the slowest output card (or, if the card is similarly synchronized with its associated device, for the slowest device) signals that it is ready for more data. When the slowest output card (external device) has timed out, the multiprogrammer responds with its data ready flag to the computer. Thus, in the timing mode, data is transmitted by the computer in synchronization with the output cards.

3-53 An important aspect of the interface between the computer and multiprogrammer is the fact that the multiprogrammer returns 13 data lines (and, of course, the data ready flag signal) back to the computer. For output modes of operation, the return lines reflect the computer data originally transmitted to the multiprogrammer and, as a result, provide an "echo" check capability for the computer. The computer, thus, can verify the integrity of its data interface paths with the multiprogrammer by comparing the data it transmits with the return data. For input modes of operation, however, return data bits 0-11 and 15 carry input data from the addressed multiprogrammer input card (external device), as described below, and cannot be used for "echo" checking.

3-54 During input modes, the multiprogrammer receives computer address words (with or without an accompanying gate signal). Note that a programmed delay is required

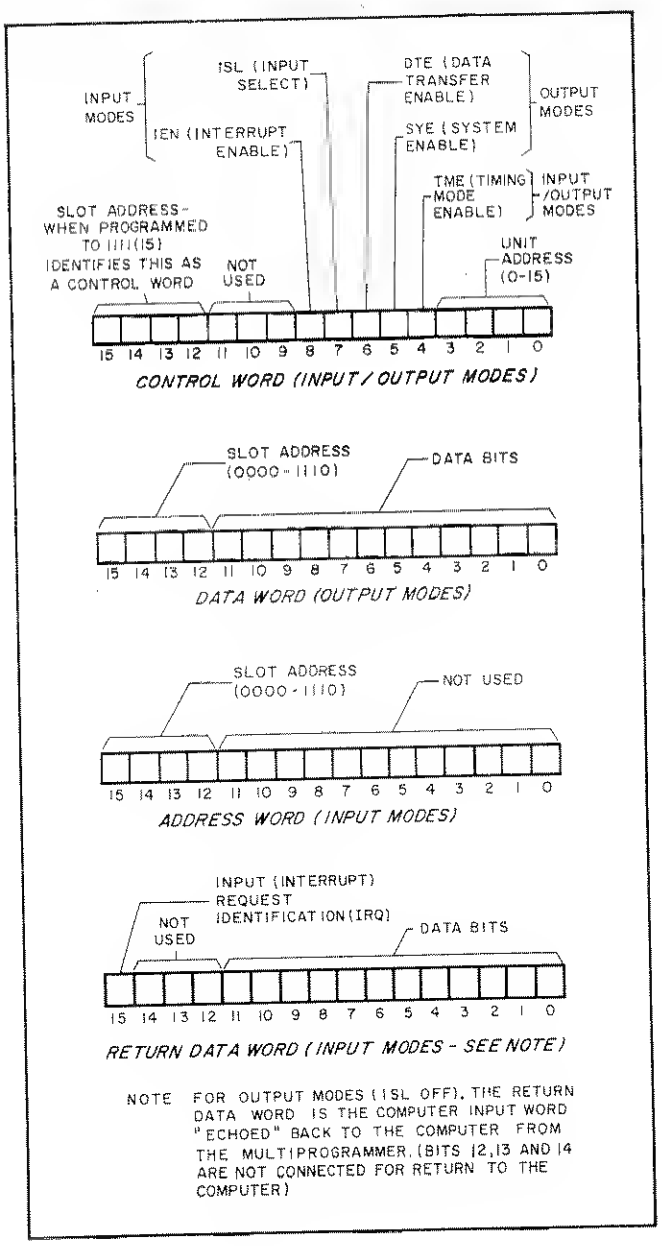


Figure 3-6. Word Formats

between addressing an input card and reading its data without an accompanying gate signal (see paragraph 3-133). Bits 12-15 of the address words identify the input card that is to transfer its data to the computer via bits 0-11 of the return data lines. Generally, two typical input modes of operation are available: one mode in which selected input cards (all or any portion) are activated and generate data ready flag signals asynchronously. That is, the computer "arms" (either individually by addressing each one with ISL on and with a computer gate or simultaneously depending upon whether a hardware jumper option is installed) the desired input cards to signal when they have data and then waits (with IEN on) for a card to signal ready. The ready

card signals the computer by enabling the multiprogrammer data ready flag to the computer. The computer responds to the data ready flag by searching for the input card (out of all that were armed) that signalled ready. The search consists of first programming IEN off and then transmitting an address word to all armed input cards in a pre-established (by software) priority until the ready card is detected (by software examination of the card's input request signal, IRQ, contained in return data bit 15).

3-55 As is discussed in more detail later in Section III, programming variations are available during the data input portion of the searching procedure. For instance, since the computer address word (which transfers the input data) need not be transmitted to the multiprogrammer with an accompanying gate signal, the addressed input card need not be reactivated for another data input cycle with its external device (card activation requires that ISL be on and the card addressed with a computer gate). Note, further, that the interrupt (data ready) search input mode requires that a certain procedure be executed by the computer during which multiprogrammer control modes are enabled and subsequently disabled. A typical search procedure is discussed in subsequent paragraphs in this section.

3-56 The other type of input mode of operation is the dedicated input mode in which the computer enables only one multiprogrammer input card to signal it is ready with data. That is, the computer maintains (in its input/output interface card which connects the multiprogrammer to the computer) the address of only one input card such that only that card is allowed to signal (via the multiprogrammer data ready flag) that is has data available for the computer. When the card signals ready, the computer can utilize the addressed input card data since it is continually present on bits 0-11 of the return data lines. Since only one card is enabled, the search process is not required, however, the input ready status of the card is returned on return data bit 15 anyway.

3-57 The dedicated input mode is, therefore, similar to the output mode of operation in that input data transfers can be done in either the handshake or timing (wait) modes of operation. As for the output data transfers, input data transfers in the handshake mode are accomplished without direct synchronization between the computer and input card (external device). In the timing mode, data input transfers are synchronized. Note, further, that similar to the interrupt search input mode, several variations are possible in the actual data input operation. That is, as in the search mode, the computer address word that reads in the input data to the computer need not be accompanied by a computer gate signal. Thus, the input card need not be reactivated for another input cycle with its external device. In fact, the computer may, at this point, address another input card and, thereby, execute the input mode with another input card (and, of course, external device). The data transfer options are not available during output modes of operation in that computer data words addressed to a multiprogrammer output card must always be accompanied by a computer gate signal which notifies the multiprogrammer output card that it may process the data word.

3-58 Control Word

3-59 A control word has two primary functions: to select a unit of the multiprogrammer system (either the 6940B master unit or one of the 6941B extender units) so that input/output cards of that unit input or receive information as specified in subsequent address or data words; and to select one or more control modes (SYE, DTE, or TME for data output transmission or ISL, IEN or TME for data input reception). Whenever the control word code is programmed (slot address 1111), the states of bit positions 0, 1, 2, and 3 (unit address); bit 4 (TME); bit 5 (SYE); bit 6 (DTE); bit 7 (ISL); and bit 8 (IEN) are stored within the 6940B.

3-60 **Unit Addressing.** The decimal equivalent of the 4-bit unit address (with bit position 3 being the most significant) corresponds directly to the assigned number of the unit being selected. When 0000 is programmed, unit ØØ is selected; when 1111 is programmed unit 15 is selected. The 6940B master unit is assigned unit number ØØ, while the 6941B extender units are numbered consecutively from Ø1 up to 15. A unit remains selected, and its input/output cards enabled, until a new unit address is programmed.

3-61 It should be noted that a unit address is decoded and stored by the 6940B each time a control word code is programmed. Therefore, when a control word is issued for the purpose of selecting a control mode (SYE, TME, DTE, ISL, or IEN) the unit address should be reissued, if it is desired to retain the same unit selection. If the unit address bits are left in the 0-state, unit ØØ will be selected.

3-62 Output Mode Control

3-63 In the multiprogrammer, output modes utilize the SYE, DTE, and TME mode control commands and are specified by the *absence* of the input select control command. When a control word with bit 7 = 0 has been received and stored in the multiprogrammer, the multiprogrammer return data lines to the computer carry the computer "echo" check data. In addition, the 12 data bits (0-11) of subsequent data words are utilized in the addressed (bits 12-15) output card.

3-64 **System Enable** (see Figure 3-7). System enable (SYE) is used primarily as part of an initial turn-on procedure. When the multiprogrammer is first turned on (and before SYE is programmed) the output circuits of all output cards are disabled; resistance outputs are shorted, voltage outputs are held at 0 volts, and digital outputs are held in the open

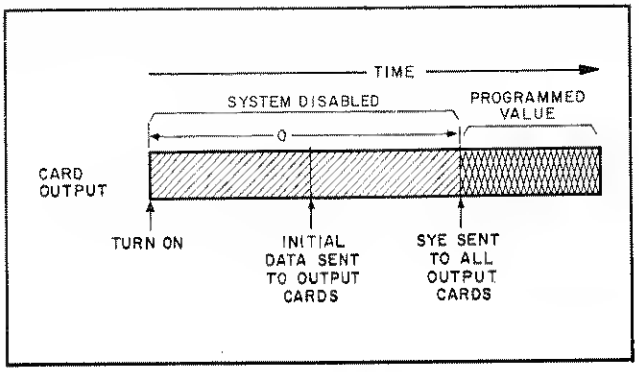


Figure 3-7. System Enable Function

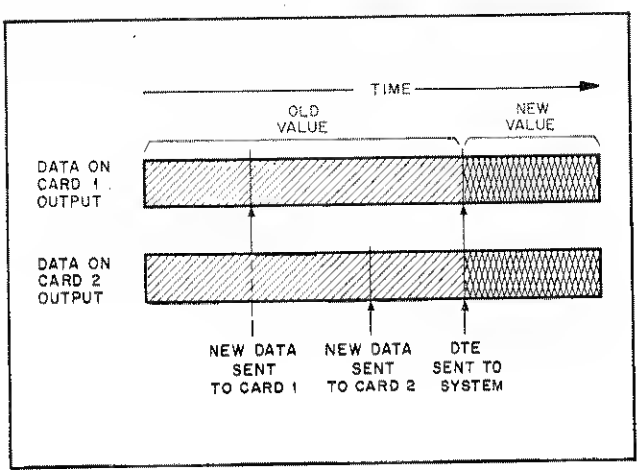


Figure 3-8. Data Transfer Enable Function

or zero state. This feature protects the external system from potentially damaging outputs resulting from the storage registers on the output cards assuming random states at turn on.

3-65 While the output circuits are still disabled, each output card can be addressed and loaded with data representing a set of initial conditions. SYE is then selected by programming bit 5 of a control word to the 1-state. This immediately activates the previously addressed cards, allowing them to develop an output proportional to the data initially stored.

3-66 In the event of a power failure in a downstream unit, an SYE flip-flop on each output card in the affected unit will be reset when power is restored. This will inhibit the card output (even though SYE from the 6940B is still on) which could go to a random value (caused by the card's storage registers going random) at turn on. In order to reinstate the card outputs, the cards must be individually re-addressed and issued new data.

3-67 For additional protection of the external system, SYE will be disabled under any of the following conditions:

a. Power failure of the 6940B

b. Setting LINE switch to OFF.

c. Removal of data input plug P1 (a jumper on P1 completes the SYE circuit internally).

d. Programming bit 5 = 0.

e. Removal of mainframe card A3 or A5 (A5 is applicable to the 6940B only).

f. Crowbar circuit activated.

3-68 Data Transfer Enable (see Figure 3-8). A data transfer enable (DTE) line is connected to all output cards in the system but is used only by output cards having dual-rank storage and by the digital (TTL) data and relay output cards. The primary function of DTE is to permit the simultaneous transfer of data from all output cards (using DTE) to the external system. DTE is selected by programming bit 6 = 1.

3-69 Output cards with dual-rank storage have two sets of storage registers. The first set of registers store the programmed data as it is entered. The second set of registers receive the data from the first set of registers and apply the data to the output conversion circuits only when DTE is programmed. For output cards with dual-rank storage, the DTE mode is normally used in either of two ways:

(1) *DTE is selected first.* The output cards are then addressed and programmed one at a time (in the normal way). Since DTE is present, the programmed data is transferred immediately from the first set of registers, to the second set of registers, to the conversion circuits. Each card, thus, produces an output proportional to the programmed data as it receives the data.

(2) *DTE is not initially selected.* The output cards are addressed and store the programmed data in the first set of registers, but do not transfer the data to the second set of registers, since DTE has not yet been programmed. This method permits the first registers of all cards to be loaded with data first; then by programming DTE the output of all the cards is simultaneously transferred to the external system. The output cards will continue to hold the most recently programmed value after DTE is removed.

3-70 The digital (TTL) and relay output cards have only a single level of storage and the outputs respond to data as the card is programmed. However, a gate line (or a contact closure available on the relay output cards) is enabled only when OTE is programmed. The gate line (or contacts) can be used in the external system to initiate two operations:

(1) To simultaneously strobe the outputs of all digital data and/or relay output cards into the external system.

(2) To start a timing flag circuit in the external system that will hold the flag line returned to the multiprogrammer in the busy state until the circuit times out. The delay provided by this circuit should coincide with the maximum time

required for the external system to process the digital data or relay outputs.

3-71 **Timing Mode.** For output, the timing mode (TME) specifies whether or not the computer data output will wait for the addressed output cards to signal ready for more data. By selecting TME (programming bit 4 = 1), the busy status of the flag control line returned to the computer is made a function of the maximum time required for the individual output cards to complete processing their last data input. Resistance, D/A voltage converter, and certain other output cards contain a monostable-type common timing flag (CTF) circuit that can be preset to any period between 10μsec and 20sec to indicate the maximum processing time for that card.

NOTE

The resistance output cards are normally supplied with a nominal 6msec CTF period to cover the operating time of the output card relays. Other CTF periods between 100μsec and 20sec can be selected by simply changing a capacitor value in the CTF circuit. CTF periods between 10μsec and 100μsec require a modification of the CTF circuit.

3-72 For relay and TTL digital output cards, the period of CTF is determined by the external system. (Details are provided in the instruction manual for the output cards.)

3-73 When an output card is addressed in the correct mode, its CTF circuit is started. If TME has been previously selected, the flag line to the computer will be held in the busy state for the period of CTF. A busy flag signals the computer not to input new data. The CTF outputs of all the cards are logically ORed together and directly control the status of the flag line in the TME mode. If TME is not programmed, the CTF circuits will still produce a timing pulse but it will not affect the flag line until TME is selected. In the absence of a TME selection, the handshake mode is automatically in effect and allows data to be entered from the computer at the maximum rate of 20k words/sec. In multiprogrammer systems employing many output channels, use of the timing mode *only* can consume substantial amounts of programming time. For example, to program a system containing 10 output cards, with each card requiring 1sec to settle, would require approximately 10sec of program time. The better approach here would be to first load the 10 output cards in the handshake mode (requiring approximately 500μsec) and then select the timing mode. Since the timing flag outputs of all the cards are logically ORed together, they will time out simultaneously in approximately 1.0005 sec. In cases where the timing flag periods differ from card-to-card, the flag line will be held busy until the longest CTF has timed out.

3-74 Input Mode Control

3-75 Input modes utilize the ISL, IEN, and TME mode control commands and are specified by the *presence* of the ISL command which must be programmed on (bit 7 = 1) at some point in the procedure for establishing either of the two basic input modes (the interrupt search or dedicated input modes). The programming of IEN, on the other hand, specifies which of the two input modes will be established. In addition, certain input cards are provided with a hardware option that allows the programming of IEN to simultaneously "arm" the cards for data input operation with their external device. The timing mode, TME, is used in both basic input modes. TME is required in the interrupt search mode but is optional in the dedicated input mode. The following paragraphs describe these functions, their interrelationships with each other, and their relationships to the output mode commands previously discussed.

3-76 **Input Select.** The input select (ISL) command provides two functions as follows. First, when programmed on, ISL enables multiprogrammer computer return data lines 0-11 and 15 to carry subsequently addressed multiprogrammer input card data on bits 0-11 and, if applicable, card input request identification (IRQ) information on bit 15. Second, for the input cards that interface (through the multiprogrammer mainframe circuits) data from an external device to the computer, ISL is used to individually activate a card (when it is addressed) for data input operations with its external device.

3-77 Data input from an external device to an input card requires that the input card's gate/flag interface with the external device and the computer (via the multiprogrammer mainframe) be activated. Input card activation can be done selectively by addressing the card in the ISL mode with an accompanying computer gate. The activation of several input cards can also be accomplished simultaneously when IEN mode is programmed by first installing a hardware option jumper on the desired cards. Figure 3-9 illustrates the timing for input card activation in the ISL mode. Input card activation with IEN is discussed in subsequent paragraphs. Notice, further, that ISL input card activation requires that the computer gate be supplied when the card is addressed and that ISL need remain on only during the actual addressing of the card.

3-78 With ISL on, input data from an addressed card (having input capability, of course) is available on the multiprogrammer's return data lines for as long as the card's address is present from the computer input/output interface card. Importantly, the computer gate is not required (and, in fact, for some cards, i.e. the relay output/readback, is not allowed) to read the card data. If the computer gate is transmitted

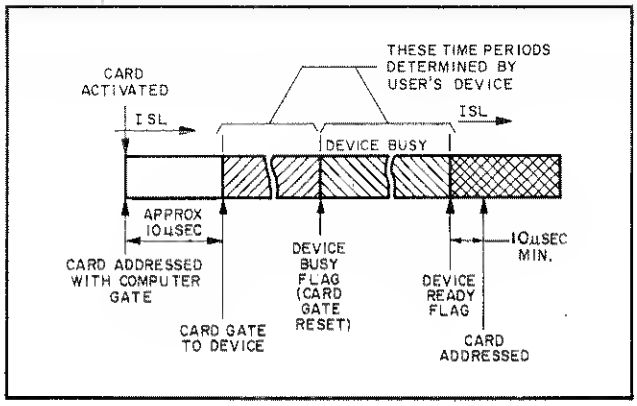


Figure 3-9. ISL Input Card Activation and Data Input

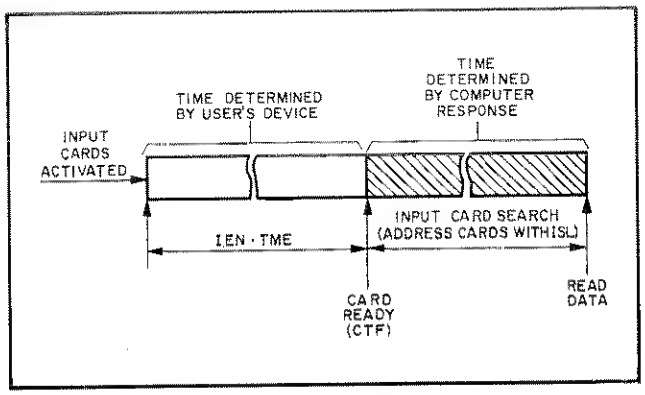


Figure 3-10. Interrupt Enable Mode Function

during data input (or subsequently), as was described in the above paragraph, an input card is activated and initiates a data input transfer cycle with its external device by generating a gate to the device.

3-79 Input cards are deactivated (control circuits on the card are reset to inhibit the card from signalling data ready) by first programming ISL off and addressing the card with a computer gate. Thus, the card remains in the deactivated state until the program reactivates the gate/flag circuits (and the card's control circuits) by addressing the card with a computer gate in the ISL mode as described in the previous paragraph.

3-80 **Interrupt Enable.** The interrupt enable mode (IEN) is used primarily to establish the interrupt search input mode of operation. In the interrupt search input mode, several (up to 240 input cards having input interrupt capability, of course, such as the digital input cards) can interface asynchronously with the computer (via the computer's input/output interface card which connects the multiprogrammer to the computer). Note that, in this mode, IEN must be accompanied by the timing mode enable (TME). The IEN command can also be used to activate a group of input cards if a hardware option is installed on the cards. This provision eliminates the need for individually addressing input cards in the ISL mode (see above) to activate them. Of course, when the jumper is not installed, input cards must be selectively "armed" for interrupt.

3-81 When IEN is programmed on (bit 8 = 1) in conjunction with TME (bit 4 = 1) after input cards have been activated, the common timing flag circuits of all activated cards are enabled (see Figure 3-10). Depending upon the external devices in use, any time after IEN is programmed, an input card (in response to its external device's flag ready signal) may enable its common timing flag to signal the computer (via the multiprogrammer flag to the computer interface card) that data is ready. The computer, thus, is requested to read (input) data from the multiprogrammer. The program can respond to an input card interrupt request in several ways as follows:

a. The program can search for the ready input card in any pre-determined priority. The program should first remove IEN (thereby preventing any other input cards from generating data ready flags should they subsequently time out), turn on ISL and then sequentially address the input cards in order to read in data. The program can determine input card readiness (interrupt requested) from bit 15 (the input request identification bit) which is also received when an input card is addressed.

b. The program can also ignore interrupts from any input card by merely not addressing the input card.

c. Further, the program can utilize a software table to determine when to accept/not accept input interrupts and, also, to establish the input search priority as a function of the system status.

3-82 If the input search is performed, the computer, after determining that it has located and read in the ready input data, can reactivate the interrupt mode (turn IEN and TME on) and wait for another input card to signal it is ready. This process is repeated, then, until the program determines that the search mode is no longer desired at which time IEN is programmed off.

3-83 As previously mentioned, IEN can also be used to activate all input cards on which a hardware jumper option to allow this function has been provided and installed. In this situation, the cards respond to IEN by activating their gate/flag interface with the associated external device so that selective input card activation in the ISL mode is not required. However, since IEN should be turned off, during the input card search (read) period after a card signals ready and turned on again after the search is over, it is possible to reactivate (when IEN is turned on again) a card that may not be expected to return data. Thus, the hardware option to activate input cards by programming IEN should be used with discretion.

3-84 **Timing Mode.** The programming of TME controls the

programmed in 2's complement form. Bit 11 is the sign bit; bits 10 through 0 control the magnitude of the output voltage.

3-93 **Relay Output Cards.** The 12 data bits control the states of 12 relays on the output cards. Programming a logical 1 in a particular bit position energizes the corresponding relay, which in turn provides an output contact closure. The data transfer enable mode is also employed on relay output cards.

3-94 **Digital Output Cards.** The 12 data bits are converted to optional logic sense and voltage polarity 12-bit outputs for use by the external device. By selecting simple option jumpers (or providing custom circuits) the user can interface the multiprogrammer with a wide variety of digital input devices. The data transfer enable mode is also employed on the digital output card.

3-95 **Relay Output/Readback Cards.** The relay output/readback cards are similar to the relay output cards in that 12-bit data from the computer controls the state of 12 relays. The relay contact closures are then outputed to an external device. The relay output/readback cards in addition, however, provide 12-bit data back to the computer in the input direction. The status of the data storage circuits that control the output relays on the card are transmitted back to the computer when the card is addressed in the ISL mode. Return data bits 0–11, then, reflect the last programmed states of the relays. Note that the address word issued to read back the data from the card must *not* be accompanied by the computer gate. The absence of the gate ensures that erroneous data will not be strobed into the storage circuits.

3-96 **Stepping Motor Card.** The stepping motor card produces a train of squarewave pulses in response to the 12 data bits. Eleven (bits 0 - 10) of the data bits control the number (1 to 2047) of pulses in an output pulse train and bit 11 determines which of two output terminals on the card delivers the pulse train.

3-97 **Bipolar Power Supply/Amplifier (BPS/A) Control Cards.** The BPS/A control cards provide resistance outputs to control the voltage output, current limit, and gain of BPS/A's. These cards are similar to the resistance output cards described in paragraph 3-91. However, in addition to providing resistance programming, the BPS/A current control card monitors the current limit status of the related BPS/A. When the current control card is addressed in the ISL mode, the current limit status is transmitted back to the computer on return data bit line 0.

3-98 Input Address Word

3-99 An address word contains the slot address (bits 15 through 12) of an input card and can be programmed to any number from 0000 to 1110. Bits 0-11 of the address word are not used in the multiprogrammer. When the addressed word contains the slot address of a card having input capability (and the unit containing that slot has been previously selected in a control word and the ISL mode is on), bits 0–11 of the input card are placed on bits 0–11 of the multiprogrammer's return data lines. In addition, bit 15 of the multiprogrammer's return data reflects the input ready/busy status of the input card, if applicable.

3-100 The significance of the data and input request identification bits returned to the computer from an input card varies with the type of card addressed. The exact meaning and applications of the return data are covered in detail in the instruction manuals for the individual cards. However, the general applications of the data bits in the digital input, event sense, voltage monitor, pulse counter, programmable timer, and process interrupt cards, are described in the following paragraphs.

3-101 **Digital Input Cards.** The digital input cards interface 12-bit TTL, DTL, or contact closure data from an external device to the computer. The 12-bit data can be positive or negative true logic sense at the option of the user and are stored on the input card when the user's flag goes ready (trailing edge). An optional jumper may be removed to disable this data storage requirement in which case the data inputs appear at the outputs as received. The data can be subsequently transferred to the computer when the card slot is addressed in the ISL mode. The digital input card contains gate/flag circuits that exchange the necessary control signals with the user's device to implement the input functions previously described. The logic sense of the gate/flag signals to/from the user's device can be positive or negative true logic and are also independently selected by the user. The digital input card also contains the hardware option (jumper W6) previously described that allows the card to be activated when IEN is programmed on.

3-102 **Event Sense Cards.** The event sense card compares the magnitude of an external 12-bit input word with a stored reference word and generates a computer interrupt for any of four conditions, depending on the placement of a jumper on the card. The four possible conditions are: In=Ref, In≠Ref, In>Ref, In<Ref. The reference word is loaded from the computer. Both the input and reference words can be read back to the computer.

3-103 The reference word is sent to the event sense card in the Handshake mode, using an output data word. Some time later, the card is armed in the input mode (ISL on) by issuing its address together with a computer gate. After arming the desired cards, the interrupt enable (IEN) and timing modes (TME) are programmed on.

multiprogrammer flag returned to the computer. With TME on (bit 4 = 1), the common timing flag (CTF) circuits of the input cards are enabled and allowed to control the multiprogrammer flag line. With TME off, the multiprogrammer flag line is controlled by the multiprogrammer's handshake flag generator which automatically generates a multiprogrammer data ready flag approximately 40μsec after the multiprogrammer receives a computer gate. The use of TME for input data transfers varies with the basic mode of input transfer desired: the dedicated input mode or the interrupt search input mode.

3-85 *Dedicated Input Mode.* This mode is established when the IEN command is off and the ISL mode is on. Further, the address of an input card is maintained by the computer in its multiprogrammer I/O interface card thereby "dedicating" the I/O interface card to the one multiprogrammer input card. If TME is also programmed, the addressed input card CTF circuits control the multiprogrammer flag to the computer such that when the associated external device signals the input card that data is available, the input card will switch the multiprogrammer flag to the ready state. Thus, the computer I/O interface card is notified that data is ready at which time it can signal (via the computer interrupt system for instance) the computer to accept the data. Data is available, then, to the computer as long as the input card address is enabled.

3-86 If TME is programmed off, the input card's CTF circuit does not control the multiprogrammer's flag to the computer. Instead, the multiprogrammer's handshake flag is substituted in which case the multiprogrammer generates a data ready flag to the computer I/O card approximately 40μsec after it receives a computer gate signal. Thus, the computer can input data from the addressed input card without regard to the gate/flag circuits of the input card or external device. Notice that if an external device flag is not supplied, the input card storage circuits should be disabled by removing a hardware jumper. With the jumper installed, the storage circuits require the trailing edge of the device flag in order to accept new data. Another way of dealing with this situation is to jumper the input card gate output to the flag input in which case the device flag will be simulated and produced as a function of the input card gate. The handshake input mode can be used as follows: The computer can program the multiprogrammer I/O card to ignore the handshake flag and rely upon software to determine when the input card has ready data (software can subsequently examine bit 15 to make this determination).

3-87 *Interrupt Search Input Mode.* In the interrupt search input mode, several multiprogrammer input cards are activated (refer to the ISL and IEN mode discussions for methods by which input cards are activated) and the IEN and TME commands are subsequently programmed on. With IEN and TME on, the CTF circuits of all activated input cards are enabled and control (individually) the multiprogrammer flag line to the computer. The first activated input card to time out (receive a data ready flag from its external device) toggles the CTF line and notifies, thereby, the multiprogrammer's I/O interface card in the computer that data is ready. The I/O interface card notifies the computer, via the computer's interrupt system, that data is ready whereupon the computer can search through all active cards (address each in turn) to determine (by examining bit 15 of the return data) which one was ready with data.

3-88 In the waiting period of the interrupt search mode, therefore, TME must be programmed on along with IEN to allow the activated input cards to control the multiprogrammer's flag line to the computer. Because of this, then, the interrupt search mode should not be programmed until all output cards have timed out. In addition, during the actual search, as previously discussed, IEN and TME should be turned off to prevent additional computer interrupts from being generated by the multiprogrammer flag line.

3-89 Output Data Word

3-90 A data word contains two types of output information; slot addresses (bits 15, 14, 13, and 12 programmed to any number from 0000 and 1110) and data (bits 11 through Ø). The decimal equivalent of the 4-bit slot address (with bit 15 being the most significant) corresponds to the slot number to be selected. When a slot is addressed (and the unit containing that slot has been previously selected) the contents of bit positions 11 through 0 are stored on the output card in the addressed slot. The data bits are used in different ways on the various type output cards and their exact applications are covered in detail in the instruction manuals for the individual output cards. However, the general applications of the data bits in the resistance, D/A voltage converter, relay output, digital output, stepping motor, and BPS/A control cards are described in the following paragraphs.

3-91 **Resistance Output Cards.** Bit positions 11 through 0 control the configuration of a 12-element precision resistance network. When a logical 1 is programmed in a particular bit position, the resistor in the network corresponding to that bit position is switched into the circuit. Programming a 0 in the same bit position short circuits the resistor. Bit 11 normally controls the state of the most significant resistance value.

3-92 **D/A Voltage Converter Cards.** The programmed data bits control a DAC module on the card which generates a bi-directional binary-weighted current proportional to the digital input. This current is applied to an operational amplifier which produces a proportional output voltage in the range of −10.240V to +10.235V. Positive values are

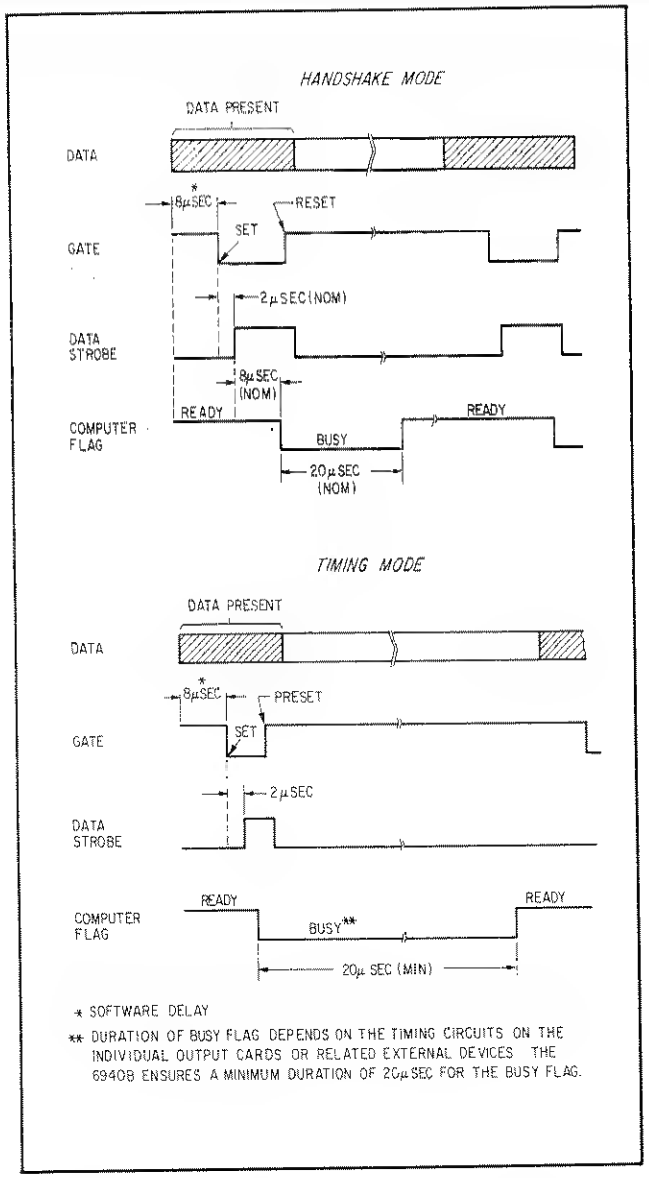


Figure 3-11. Data Output Modes, Timing Diagram

programmer input operation is complete, and the computer immediately responds by resetting the gate line. When the gate line is reset, the multiprogrammer resets the flag to the ready state. A circuit within the multiprogrammer holds the flag busy for 20μsec. The computer may input new data any time after the flag line goes to the ready state.

3-113 **Timing Mode.** The initial phases of the input operation (up to strobing the data into storage and resetting the gate line) are essentially the same for both the handshake mode and the timing mode. The key difference between the two modes is control of the flag line. In the handshake mode the flag line is automatically reset to the ready state when the gate line is reset, and in no way reflects the status of the output cards. In contrast, the timing mode flag is held busy (20μsec minimum) until timing circuits on previously addressed output cards have all timed out, indicating the readiness of the output cards to accept new data. The timing mode is covered in detail in Paragraph 3-71.

NOTE

In either data output mode, the computer requires an indication (via the ready-to-busy transition of the flag line) that the multiprogrammer has completed storage of its last data input. Until it receives this signal, the computer should not reset the gate line or input new data. For this reason, if a non-existent unit is addressed the computer will not receive a flag transition so that the multiprogrammer system may, consequently, lock-up (data ready flags may not get through to the computer's system software). A similar situation exists if a unit is addressed and it has not been turned on. In the latter case, the problem is compounded further since any units further down-stream from the deenergized unit will also be disahled, and addressing any one of these may also cause the multiprogrammer system to lock-up. In addition, the deenergized unit will return an erroneous flag indication to the computer. It is important, therefore, to make sure that all units are turned on before starting-up the system and, in addition, to provide a system software loop to verify that the multiprogrammer system has not locked up.

3-114 Data Input Modes

3-115 Typically, the computer inputs data from multiprogrammer input cards in either of two basic modes of operation: The interrupt search input mode or the dedicated input mode. The basic modes are defined by the computer's use of the multiprogrammer's I/O interface card housed in the computer. In the search mode, for instance, the computer I/O card is not associated with any individual multiprogrammer input card but, instead, asynchronously interfaces the computer with previously-activated input cards as they become ready for data transfers from their associated external device. In the dedicated input mode, on the other hand, the computer's I/O card is "connected" to one specific multiprogrammer input card in that the input card's address must continually be stored in the computer I/O card for input data transfers from the input card to proceed.

3-116 Figure 3-12 is a timing diagram that illustrates the relationships of signals exchanged between the computer

3-104 If an interrupt occurs on an armed card, the card signals the computer of this condition via a transistion of its $\overline{CTF}$ line. The computer may now search for the interrupting card by polling (addressing) each input card individually. (Polling is normally done without the use of a computer gate). As each card is addressed, it places the 12 bits from the associated external device on the multiprogrammer backplane for read-back to the computer. As each word is read back, the computer examines the state of bit 15 of that word. Any card having an interrupt condition will cause bit 15 (via the $\overline{IRQ}$ output of the card) to be a logical 1. The computer should accept the 12 return data bits only when bit 15 of the word is a logical 1. The reference word currently stored on the interrupting card can be read back to the computer in the input mode by re-addressing the card and issuing a computer gate. Detailed programming instruction for the event sense cards are provided in the 69434A instruction manual.

3-105 **Voltage Monitor Card.** The voltage monitor card monitors dc voltages in the +10.235V to −10.240V range and returns a 12-bit binary word to the computer to indicate the magnitude and sign of the measured voltage. When the card is addressed and a gate is received (with ISL mode off), the dc voltage is converted to an equivalent 12-bit word and stored on the card. The 12-bit word is returned to the computer when the card is addressed (without a gate) in the ISL mode.

3-106 **Pulse Counter Card.** The pulse counter card counts (up or down) pulses or contact closures in the 0 to 4095 range. An output data word (ISL off) addressed to the card and accompanied by a gate loads an initial count into the counter or sets it to zero. When the card is addressed without a gate and ISL is on, the quantity (bits 0 - 11) in the counter is returned to the computer.

3-107 **Programmable Timer Card.** The programmable timer card operates as an output card, however, it also has interrupt enable capability. The programmable timer card generates a single crystal controlled pulse each time it is commanded by the program. The duration of the pulse (time interval) is the product of two factors: (1) the number of programmed time increments (from 1 to 4095); and (2) the selected period (jumper on card) of the increments in any one of six decade values ranging from 1μsec to 0.1 sec. Output data word bits 0 - 11 determine the number of time increments. The programmable timer card can be armed to provide a computer interrupt when the time interval terminates. Operation in the interrupt mode is similar to that previously described for the event sense card. Detailed programming instructions for the programmable timer card are provided in the 69600A Instruction Manual.

3-108 **Process Interrupt Card.** The process interrupt card monitors 12 external TTL or open collector logic circuits and interrupts the computer when any one or more of the circuits changes state. The interrupt can be generated by a positive-going logic transition (low to high), or a negative-going logic transition (high to low), or either, depending upon the physical connections of the monitored signals to the card. When a change of state is sensed, the card will interrupt the computer immediately if the interrupt system is turned on or the next time the interrupt system is turned on. When polled, the interrupting card will send back $\overline{IRQ}$ along with a logic one corresponding to each bit change that was sensed. Operations in the interrupt mode are similar to those previously described for the event sense card. Detailed programming instructions for the process interrupt card are provided in the 69436A Instruction Manual.

3-109 Data Output Modes

3-110 Computer data is transmitted to the multiprogrammer in either the handshake mode or the timing mode. Unless the timing mode is specifically programmed by bit 4 = 1, the handshake mode is automatically in effect. In both modes, the data output operation is coordinated by an input gate line from the computer and a flag line from the multiprogrammer back to the computer. A timing diagram for both modes is given in Figure 3-11. The timing schemes shown match the standard interface configuration covered in Section II. However, any timing scheme conforming to the following rules will operate properly.

a. Data must be present on the interface lines when the computer sets the gate line. The program must delay setting the computer gate until 8μsec after the output data bits are present on the interface lines (see paragraph 3-133). This delay allows the lines to settle before the data bits are strobed into the multiprogrammer.

b. Data must be held on the interface lines until after the gate is reset (multiprogrammer data strobe is removed).

c. The gate line must be reset while the flag is busy. (This operation is done automatically in the standard interface configuration by the computer I/O card.)

d. The computer may input new data when the flag is ready.

3-111 **Handshake Mode.** In the handshake mode, the entire input operation is completed within 50μsec.

3-112 Eight microseconds after the computer has data available on the 16-input lines to the multiprogrammer, it sets the gate control signal. Upon receipt of this signal, the multiprogrammer waits approximately 2μsec and then strobes the data into storage. Approximately 10μsec after receipt of the gate signal, the multiprogrammer sets the flag line back to the computer from the ready to the busy state. This transition signals the computer that the multi-

and the multiprogrammer and between typical input cards (the digital input card is used for the example) and their associated external device. Note that the timing diagram presents typical data transfer operations in order to depict the exchange of signals between the computer, multiprogrammer, and external device. No attempt has been made to define all possible interface variations as they will depend on the particular input cards and external devices employed. The intent is to describe general requirements for interfacing through the multiprogrammer while still depicting the broad flexibility built into the multiprogrammer and its input cards. Note that in the timing diagram negative true logic is assumed for the external device gate and flag signals.

3-117 **Interrupt Search Input Mode.** In this mode of operation (Figure 3-12A), the computer interfaces (through its multiprogrammer I/O interface card) with several (up to 240) multiprogrammer input cards. The computer interface is "free-wheeling" in that the computer activates input cards, waits for them to signal the multiprogrammer I/O card that they are ready with data, and (in response to an interrupt request by the I/O card) then searches through all activated cards to determine which of the input cards has data ready.

3-118 The search mode is initiated when the program activates the desired group of input cards. Card activation can be individually accomplished in the ISL mode (with IEN and TME off) by addressing each card with a computer gate. Note that if the hardware option jumper previously described is installed, the cards can be also activated in a group when IEN is programmed on. Assuming the jumper is not installed, I.B. of the timing diagram (Figure 3-12A) illustrates the signals generated when an input card is activated. When the card is addressed with the computer gate, the gate is enabled and causes the multiprogrammer to generate its data strobe (delayed 2μsec from the computer gate). The data strobe signal is used in the multiprogrammer to switch its flag signal to the computer into the busy state. Also, the data strobe is further delayed on the input card and used to initiate the input card's gate signal to the external device. Notice that since the card has been addressed and ISL is on, the input card's data is applied to the computer via the multiprogrammer's return data lines (the computer should ignore the data, however, as discussed below).

3-119 The multiprogrammer's data strobe causes the flag signal to the computer I/O card to switch to the busy state. The I/O card thereupon resets the gate signal to the multiprogrammer which responds by resetting its data strobe (and input card delayed data strobe) and, therefore, switching its flag line to ready. Note that TME must be off to allow the multiprogrammer to generate its handshake flag in response to the data strobe (which follows the computer gate). Further, the computer's interrupt system should be programmed to ignore the ready transition of the handshake flag and, thereby, prevent the computer (by not generating an interrupt) from accepting erroneous data.

3-120 At some time after the transition of the input card gate to the external device, the device should switch its flag input to the card into the busy state. Flag busy (leading edge) can reset the gate line on the input card. Thus, with all external devices timing out (the activation process is repeated for all desired input cards), the computer can enter the interrupt enable mode by turning IEN and TME both on. With these control modes on, the multiprogrammer flag to the computer is controlled by the common timing flag (CTF) output of each input card. The I/O card will wait and respond to the first input card that signals it has data ready from the external device. Note that the point at which the interrupt mode is enabled can occur at any time after the input cards are activated. The interrupt mode need not wait for the external devices to signal busy. In fact, the interrupt mode can be enabled after an external device (or all devices) has gone busy and back to ready again. The ready state of the external device is stored on the input card.

3-121 With IEN and TME on, the multiprogrammer flag to the computer is controlled by the input card's common timing flag (CTF) output. Notice, in addition, that the computer gate (and, therefore, the multiprogrammer data strobe and input card delayed data strobe) is continually enabled on the computer I/O card.

NOTE

Since the CTF line is used to signal when an input card is ready for data transfer, all multiprogrammer output cards should be allowed to time out before enabling the interrupt mode. This will prevent an output card from unintentionally generating a CTF interrupt during the input mode.

3-122 When the first external device has data ready, it switches the flag input to the input card to the ready state (trailing edge). The device flag-ready transition causes the input card to enable its CTF output which switches the multiprogrammer flag to the computer to the busy state. The multiprogrammer busy flag resets the computer gate on the I/O card which, in turn, resets the multiprogrammer data strobe. The input card delayed strobe is also reset which causes the input card to reset its CTF output and, as a result, the multiprogrammer flag to the computer is switched to the ready state.

3-123 The ready transition of the multiprogrammer flag is

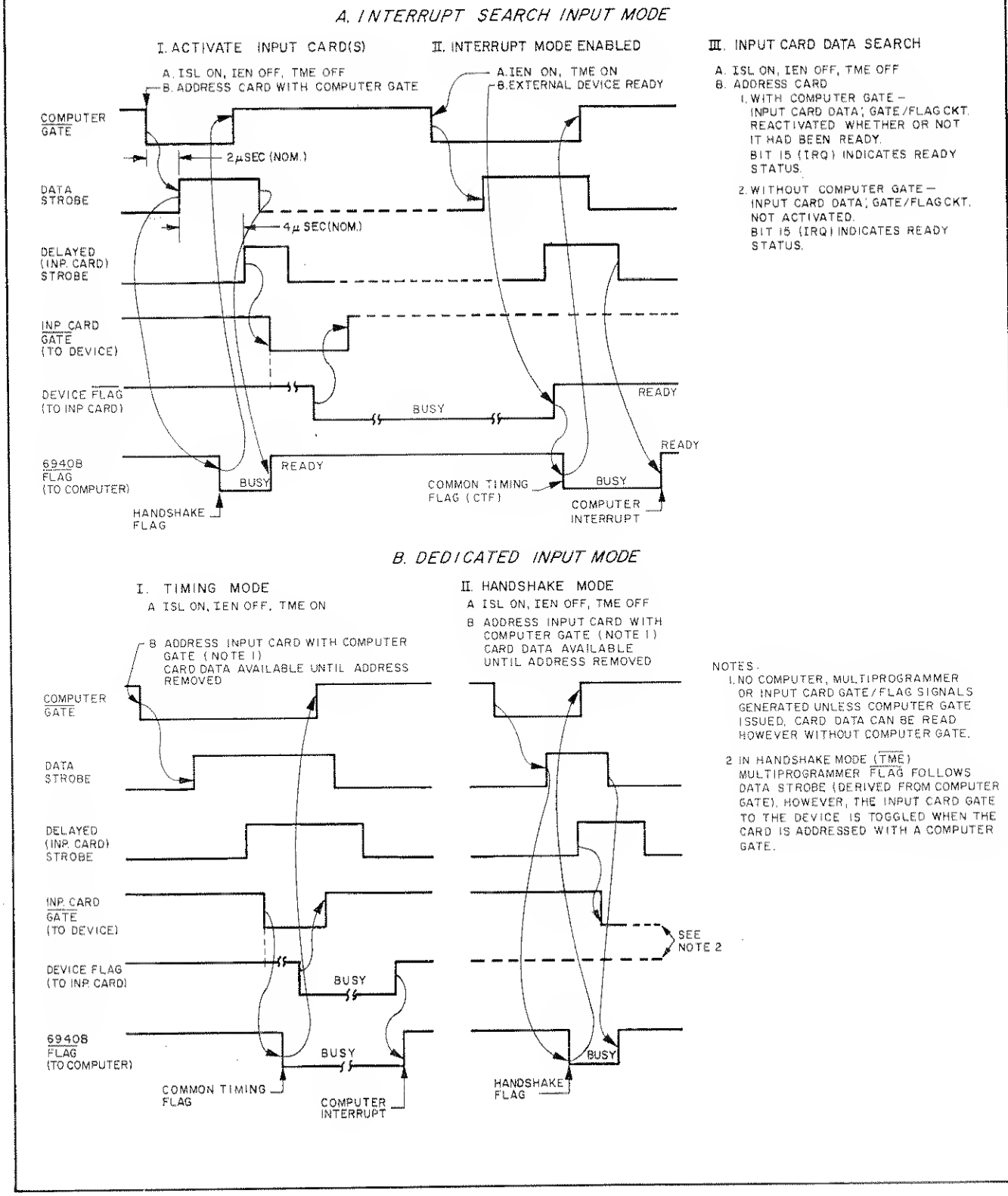


Figure 3-12. Data Input Modes, Timing Diagram

100 feet of cabling between each unit. A fully complemented system (a computer, one 6940B, and fifteen 6941B's), with the maximum distance between each unit, utilizes 1600 feet of cabling. The programmed delays must be sufficient to accommodate the worst case condition (1600 feet of cabling). A delay is required for all output data transfers (computer to multiprogrammer system). Delays are also required when data is readback to the computer from the multiprogrammer system without an accompanying gate signal.

3-135 **Output Transfer Delay.** A delay of 8μsec must be programmed between data output to the multiprogrammer and setting the gate signal. The delay allows the output lines to settle before the data is strobed into the multiprogrammer. The 8μsec delay applies to all data output transfers (control, data, and address words) requiring a gate regardless of the unit number of the multiprogrammer receiving the data.

3-136 **Readback Delay (Without Gate).** A programmed delay must be incorporated between addressing (address word) an input card and reading its data without a gate. If the address word is part of an input card data search (see paragraph 3-117), the delay time depends on the multiprogrammer unit number (0-15) of the addressed input card. The delay (wait time) allows the addressed input card time to respond and also allows the address lines time to stabilize before the data is accepted. The following delays (wait times) are used for multiprogrammer unit numbers 0-15.

Unit Number	Delay (wait time) *
0, 1	12μsec
2, 3	15μsec
4, 5	20μsec
6, 7	24μsec
8, 9	28μsec
10, 11	32μsec
12, 13	36μsec
14, 15	40μsec

* For maximum distance of 100 feet between units.

3-137 Sample Programs

3-138 The following paragraphs provide simple programming examples written in HP Assembly language for outputting data from the computer to the multiprogrammer and for reading data from the multiprogrammer to the computer. The sample programs are for illustration purposes only and do not reflect all ways in which the multiprogrammer can be programmed. For instance, the program continually tests if the multiprogrammer is ready for another word by sensing its computer I/O card Flag. The computer interrupt system can also be utilized for this function by allowing the multiprogrammer program to be called via the interrupt system when the next word is ready for transfer.

3-139 Output Data to Multiprogrammer Output Card (Unit ØØ, Slot ØØ)

INSTRUCTION	FUNCTION
.	
.	
.	
LDA OUTCW	Load A Reg. with 17Ø16Ø; Control word to set multiprogrammer to SYE DTE, and TME modes, select unit ØØ
OTA MP	Output control word to multiprogrammer's computer I/O card.
NOP	
NOP	Wait 8μsec for output lines to
NOP	settle
NOP	
STC MP' C	Set Gate to multiprogrammer; reset I/O card Flag
SFS MP	Check if multiprogrammer ready for next word (I/O card Flag set)
JMP *-1	Multiprogrammer not ready yet; loop until ready
LDA OUTDW	Multiprogrammer ready. Load A Reg with ØØ7777; set slot ØØ to all ones
OTA MP	Output data word to multiprogrammer I/O card.
NOP	
NOP	Wait 8μsec for output lines to
NOP	settle
NOP	
STC MP, C	Set Gate to multiprogrammer; reset I/U card Flag.
SFS MP	Check if multiprogrammer ready for next word
JMP * -1	Multiprogrammer not ready yet; loop until ready
.	
.	
.	

3-140 The sample output program above illustrates several important considerations in programming output cards. One, the multiprogrammer requires a computer Gate (8μsec after data is present on output lines) for each control and data word it receives from the computer. Also, the multiprogrammer must be set to the correct programming mode prior to transmitting the data to the desired output card. The correct mode, of course, will depend on system considerations. However, notice that before the data word was sent to the output card, the multiprogrammer was set to the SYE, DTE, and TME modes. With SYE on, the data from the card is available to the external device. With DTE on, if the card is a dual-rank storage card, it appears to have single-level storage so that the output data appears immediately at

a signal to the computer I/O card (which must be previously programmed to respond to the ready flag) to generate an interrupt request to the computer. When the computer honors the request, the program must search for the input card (or cards) that have input data ready. The input card data search requires that ISL be programmed on and IEN and TME off (to prevent further interrupts from occurring). Each active card is addressed in a software-determined priority in order to read in the data (bits 0-11) and input card request identification (bit 15) on the multiprogrammer return data lines. The program examines bit 15 to determine if the card data bits represent valid data. Upon identifying the input ready card, the program can search for other ready cards or it can reenable the interrupt mode and wait for the I/O card to generate an interrupt request again in response to an input card CTF ready flag.

3-124 After a data ready card has been read, it should be reactivated (if more data is expected) or de-activated. The card is reactivated again by addressing it in the ISL mode with a computer gate. The input card can be de-activated (prevented from generating further input interrupt requests) by addressing the card with a computer gate but with ISL turned off. This will reset control circuits on the input card needed to keep the card activated.

3-125 Notice that when the W6 IEN jumper is in use, a ready input card is automatically reactivated when IEN is programmed on. Further, any input cards that were purposely de-activated prior to enabling the interrupt mode, will as a result be reactivated when IEN is programmed back on. Input cards, however, that are in the busy state are not affected when IEN is programmed on.

3-126 **Dedicated Input Mode.** In this input mode (see Figure 3-12B), the computer interfaces (through its multiprogrammer I/O card) with one multiprogrammer input card and its external device. Input data transfers with an input card continue as long as the address of the card is placed in the storage circuits of the computer I/O card. Input data transfers, further, can be executed in the timing mode or in the handshake mode with transfers in the timing mode providing for close synchronization among the computer (and its I/O card), the multiprogrammer (and its input card), and the external device.

3-127 *Timing Mode.* In the timing mode (ISL on, IEN off, and TME on), the multiprogrammer flag to the computer is controlled by the addressed input card's CTF output. The card is activated with a computer gate which initiates the multiprogrammer data strobes and input card gate to the external device. Since the card address remains enabled (it is stored in the computer I/O card), the input card CTF output also causes the multiprogrammer flag to the computer to switch to the busy state. This causes the computer gate to reset thereby resetting the multiprogrammer data strobe.

3-128 Sometime after the input card gate to the external device was enabled, the device flag to the input card must switch to the busy state. The leading edge (busy) of the device flag can reset the input card gate to the device and the input cycle now waits for the external device to signal that it has data ready. When ready, the external device switches its flag to the ready state (trailing edge) which causes the input card's CTF output (assuming the card's address is still stored in the computer I/O card) to switch the multiprogrammer flag to the ready state.

3-129 If the computer interrupt system is utilized, the transition of the multiprogrammer flag to the ready state causes the I/O card to generate an interrupt request to the computer. The computer is thus notified that data is ready from the input card. Since the input card's data (including bit 15, the input request identification bit) is continually sent to the computer I/O card as long as ISL is on and the card is addressed, the computer has immediate access to the data. The input card can be activated again with a computer gate or it can be deactivated by resetting its control circuits (addressing the card with ISL off and with a computer gate) or by removing its address from I/O card storage.

3-130 *Handshake Mode.* In the handshake mode (ISL on, IEN and TME off), the input data transfer cycles are not as closely coordinated as in the timing mode in that the multiprogrammer's flag to the computer is not controlled by the input card. With TME off, the input card CTF output is inhibited and the multiprogrammer's handshake flag controls the flag line to the computer. An example of how the handshake mode might be used for data input is discussed below.

3-131 The program can activate an input card by addressing the card with ISL on and with a computer gate. The computer's I/O card, further, could be programmed to ignore the handshake flag returned to the computer by the multiprogrammer during card activation.

3-132 After activation, the input card gate/flag interface with the external device continues as previously described. The computer can subsequently address the card (without a computer gate for example) and read in the card's data including bit 15. By examining bit 15, the computer can determine if the card's external device has inputted ready data to the card. If it had, the computer can reactivate the card as above and repeat the cycle. Note that the time at which the program "looks" (by addressing the card) at an input card to determine if it has data ready is determined by software as the card's CTF line is inhibited and cannot generate a multiprogrammer flag.

3-133 Software Delays

3-134 Software delays must be incorporated because the Multiprogrammer System is designed to operate with up to

the output of the card. For output cards that generate a Gate to the external device, DTE enables the card's Gate circuit. Finally, TME sets the multiprogrammer to the Timing Mode such that its Flag back to the computer I/O card is controlled by the output card's Flag circuits. Note that when output cards that produce Gate signals to their associated devices are utilized, DTE should be programmed on whenever TME is programmed on. This requirement is based on the fact that when TME is on, the computer waits for the multiprogrammer Flag to signal when it is ready for another word. Thus, if DTE is off, the card's Gate output is disabled so that the external device's Flag input to the card will not be received. As a result, the computer program will be in a "hung up" state in which it continues to wait for the multiprogrammer Flag to indicate it is ready. If this state is inadvertently programmed, the multiprogrammer Gate should be turned off (with a Clear Control, CLC, instruction) before reprogramming the correct multiprogrammer control mode (i.e. before either turning DTE on or TME off).

3-141 Input Data from Multiprogrammer Input Card (Unit ØØ, Slot Ø1)

INSTRUCTION	FUNCTION
⋮	
LDA INCW	Load A Reg. with 17Ø26Ø; control word to set multiprogrammer to SYE, TME, and ISL mode, select unit ØØ.
OTA MP	Output control word to multiprogrammer's I/O computer card.
NOP	
NOP	Wait 8μsec for output lines to
NOP	settle.
NOP	
STC MP, C	Set Gate to multiprogrammer; reset I/O card Flag.
SFS MP	Check if multiprogrammer ready for next word (I/O card Flag set).
JMP * -1	Multiprogrammer not ready yet; loop until ready
LDA OUT AW	Multiprogrammer ready. Load A Reg. with Ø1xxxx; address input card slot Ø1 in unit ØØ.
OTA MP	Output address word to multiprogrammer I/O card.
NOP	
NOP	Wait 8μsec for output lines to
NOP	settle.
NOP	
STC MP, C	Set Gate to multiprogrammer; reset I/O card Flag. Activate input card.
SFS MP	Check if multiprogrammer ready to input next word.
JMP *-1	Multiprogrammer not ready yet; loop until ready.
LIB MP	Multiprogrammer ready. Load B Reg. with input card data.
STC MP, C	Set Gate to multiprogrammer; reset I/O card Flag. Reactivate input card (I/O card still has card's address word).
SFS MP	Check if multiprogrammer ready to input next word.
⋮	

3-142 The sample input program above illustrates several important aspects of programming multiprogrammer input cards. First, notice that the multiprogrammer must be set to the input mode (ISL on) before input card data can be read. This control word, of course, requires the multiprogrammer Gate. Next, notice that the input card is first activated by addressing the card with a multiprogrammer Gate. When the card is ready to input data, it causes the multiprogrammer Flag to be generated and the program advances to the read-in (LIB) section. After reading the input data, the multiprogrammer Gate is again set and the input card reactivated. When the card is next ready to send data, it will again set multiprogrammer Flag and the input cycle will be repeated. It is important to note that after the input card has been addressed, the set Gate and Sense Flag process could be deleted in that input cards can be read without setting the multiprogrammer Gate. Note, that a programmed delay is required between addressing an input card and reading its data without a Gate (see paragraph 3-133). Output cards, however, require the multiprogrammer Gate as a signal to start processing a data word. Similarly, the multiprogrammer requires the Gate to notify it that it can process multiprogrammer control words from the computer. One final note, the input example shown depicts a simple "dedicated" input mode of operation. The multiprogrammer can also be operated in the input search mode in which many input cards are activated simultaneously.

3-143 LOCAL PROGRAMMING

NOTE

When the 6940B is connected to a computer, the computer must be turned on, even for local operation of the 6940B. The I/O circuits of a deenergized computer will load the multiprogrammer's I/O data lines and prevent normal operation.

3-144 Local programming is selected by setting the LINE switch to the ON position and then pressing the REMOTE/LOCAL switch. The LED in the REMOTE/LOCAL switch extinguishes to indicate that the multiprogrammer is in local.

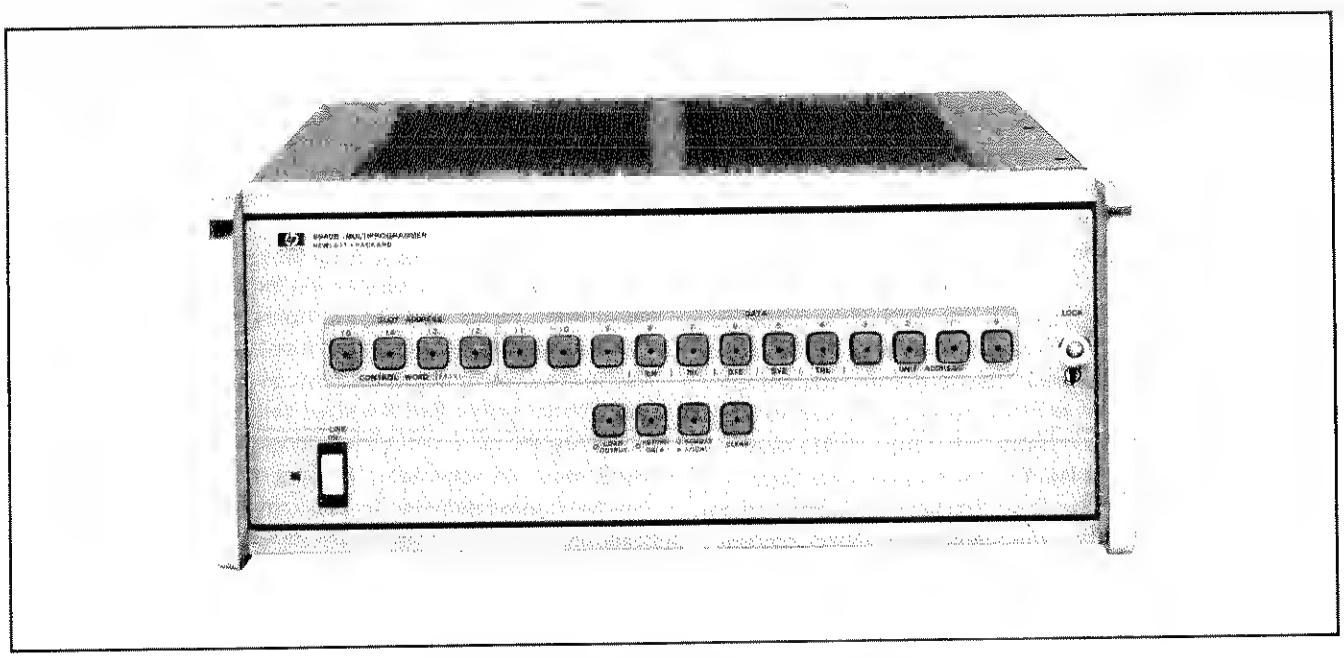


Figure 3-13. 6940B Multiprogrammer Control Panel

NOTE

When local programming is selected for the first time after the power is turned on, all 16 of the LEDs in the bit programming switches light to serve as a circuit test. The LEDs remain on until cleared or until their bit states are changed by pressing the associated switches.

When local programming is selected, control of the multiprogrammer is a function of the state of the input select (ISL) mode (that is, multiprogrammer local control is different for output and input modes).

3-145 Output Mode Local Programming

3-146 With ISL off, control of the system is transferred to the 16 bit-programming switches (0 through 15) and the three control function switches (CLEAR, LOAD OUTPUT, and RETURN DATA) of the 6940B switch register. Note that the signals that control the switch register LEDs are taken from the output of the remote/local card so that when an LED lights in response to its associated switch being pressed, it not only indicates that a logical 1 has been programmed in that bit position, but it also indicates that the switch register and remote/local selection logic associated with the bit are functioning properly.

3-147 The 16 bit-programming switches are used to develop control and data words for output mode programming of the multiprogrammer system. The definitions and functions described for control and data words used in remote programming (Paragraphs 3-58 and 3-89) apply equally to local programming.

3-148 Once a control or data word has been developed using the bit-programming switches, the operator may enter the word into the multiprogrammer system by pressing the LOAD OUTPUT switch. An LED within the LOAD OUTPUT switch lights while the switch is pressed to indicate that the command has passed through the remote/local selection logic. Before programming a new word, the bits not related to the new word must be cleared to the 0-state (associated LED off). This can be accomplished by pressing the applicable switches (the bits that are 0 in the new word) a second time or by pressing the CLEAR push-button to reset the entire 16 data bits. Next, the desired bit switches of the new word are pressed to set them to the 1-state. Note that the CLEAR switch LED is permanently connected across 5 volts dc and is always on.

3-149 The bit patterns set on the switch register are also returned to the computer I/O card via the return data lines. As each switch is pressed, its new state appears at the I/O card. When the RETURN DATA switch is pressed, it generates a flag, which signals the computer that data is available on the return data lines. An LED within the RETURN DATA switch lights while the switch is pressed to indicate that the flag has passed through the remote/local selection logic.

3-150 When REMOTE operation is again selected, the bit-programming switch LEDs indicate the bit patterns of the input computer words, and the LOAD OUTPUT and RETURN DATA switch LEDs indicate the status of the computer gate and multiprogrammer flag lines, respectively.

3-151 The switch register stores the last manual data entry so that when LOCAL operation is again selected, that entry appears on the bit-programming switch LEDs.

3-152 Input Mode Local Programming

3-153 With ISL on, local control of the system is limited to the address bits (12-15) of the switch register and the CLEAR, LOAD OUTPUT, and RETURN DATA control functions. These switches are used and operate in the same manner as described above when ISL is off (note, further, that RETURN DATA provides an additional function when ISL is on as described below). Thus, address bit switches 12-15 are used to select an input card slot, the LOAD OUTPUT switch is used to simulate the computer gate input, and the RETURN DATA switch is used to simulate the multiprogrammer flag to the computer (as well as the function described below). Similarly, the CLEAR switch is used to reset all of the address bits at one time.

3-154 Unlike output mode local programming, however, when ISL is on, switch register LEDs 0-11 are not controlled by switch register bit switches 0-11. Instead, the bit switches are disabled and the LEDs are controlled by the data from the addressed (bits 12-15 of the switch register) input card. Thus, the operator can read an input card by programming a control word with ISL on and then programming the address of the input card slot, whereupon the input card data controls the bit 0-11 switch register LEDs. An input card data bit at logical 1 turns on the associated switch register LED while a logical 0 turns the LED off.

3-155 With ISL on, in addition, the RETURN DATA LED is controlled by either the RETURN DATA switch (in which case, as in output mode local programming, the LED displays the simulated multiprogrammer flag generated when the switch is pressed) or the input request signal (IRQ) from the addressed input card. Thus, the operator can determine if an activiated input card's gate/timing circuits are responding by programming ISL on, addressing the card, pressing LOAD DUTPUT, and then observing the RETURN DATA LED. When the input card assumes the data ready state (IRQ is logical 1) the RETURN DATA LED is turned on. Conversely, RETURN DATA is off when the card is the busy state (IRQ is logical 0).

3-156 Typical Output Programming Sequence

3-157 A typical output programming sequence describing the use of control and data words, the three applicable output control modes (SYE, TME, and DTE) and the two data output modes (handshake and timing) is provided in Table 3-1. With the exception of the initialization procedure, the programming sequence does not have to follow the order given in Table 3-1.

Table 3-1. Typical Output Programming Sequence

TYPE WORD	PROGRAMMED WORD																FUNCTION
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	INITIALIZATION																
										DTE		SYE		TME			
Control	1	1	1	1	x	x	x	x	x	1	0	0	0	0	0	0	Select unit ØØ to begin initialization of output cards; all output cards disabled by SYE = 0; data entered in handshake mode (TME = 0). DTE = 1 initializes both registers of dual rank storage.
	Slot Addr.				Not Used									Unit Addr.			
Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initialize output of slot ØØ, unit ØØ. (Initial value can be other than 0.)
	Slot Addr.									Data							
Data	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Initialize output of slot Ø1, unit ØØ.
								⋮									⋮
Data	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Initialize output of slot 14, unit ØØ.
Control	1	1	1	1	x	x	x	x	x	1	0	0	0	0	0	1	Select unit Ø1 to begin initialization of its output cards.

Table 3-1. Typical Output Programming Sequence (Continued)

TYPE WORD	PROGRAMMED WDRD																FUNCTION
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initialize output of slot ØØ, unit Ø1.
																	(Initialize all output cards in system)
											SYE						
Control	1	1	1	1	x	x	x	x	x	0	1	0	0	0	0	0	Select system enable by SYE = 1; all output cards go to initial value.
							PRDGRAMMING										
Data	0	0	0	0	0	0	1	1	0	1	0	1	1	0	1	1	Data bits 11 through 0 addressed to slot 00, unit ØØ, (data shown is arbitrary value); data entered in handshake mode.
Data	0	0	0	1	0	1	1	1	0	1	0	0	1	1	0	1	Data bits addressed to slot Ø1, unit ØØ.
Data	1	1	1	0	0	1	1	0	1	1	0	1	1	0	1	1	Data bits addressed to slot 14, unit ØØ.
												SYE					
Control	1	1	1	1	x	x	x	x	x	0	1	0	0	0	0	1	Select unit Ø1 for programming; retain SYE=1 to hold system enabled.
Data	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	1	Data bits addressed to slot ØØ, unit Ø1.
																	(Continue programming output cards)
											SYE	TME					
Control	1	1	1	1	x	x	x	x	x	0	1	1	x	x	x	x	Select timing mode by TME=1; retain SYE=1. Flag line to computer held in BUSY state until longest timing circuit of previously addressed card times out.
							DATA TRANSFER (DTE)										
Data	0	1	0	1	0	0	1	1	0	0	1	1	1	1	0	1	Data bits addressed to slot Ø5, unit ØØ (slot Ø5 arbitrarily selected as containing an output card with dual-rank storage); data bits stored in first level registers of output card; output of card remains unchanged.
Data	1	1	1	0	0	1	0	1	1	0	1	1	1	0	1	1	Data bits addressed to slot 14 (containing dual-rank storage output card); output remains unchanged.
											DTE	SYE					
Control	1	1	1	1	x	x	x	x	x	1	1	0	0	0	0	0	Output of cards in slots Ø5 through 14 of unit ØØ simultaneously go to programmed values.

3-158 Typical Input Programming Sequences

3-159 Typical input programming sequences describing the use of control and address words and the three applicable input control modes (ISL, IEN, and TME) are provided in Tables 3-2 and 3-3. These programming sequences show typical examples and, as such, are not meant to be definitive of all methods of input programming. As previously indicated, many operational variations (such as, for instance, using the handshake flag, TME = 0, when interfacing with a single input card) are possible depending upon the user's requirements and specifications.

3-160 SAFETY FEATURES

3-161 Several safety features are built into the 6940B to protect the user's system from outputs that may not truly represent intentionally programmed data. Each feature is described in the following paragraphs.

3-162 SYE Override

3-163 As described previously, SYE has control over the output circuits of all output cards in the multiprogrammer system. SYE will be removed and the output cards disabled

Table 3-2. Typical Interrupt Search Input Mode Programming Sequence

TYPE WORD	PROGRAMMED WORD															FUNCTION
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								INITIALIZATION									
Control	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Select unit ØØ to initialize system; turn off all functions (particularly output functions).
								PROGRAMMING									
								1. Input card activation									
								IEN ISL				TME					
Control	1	1	1	1	x	x	x	0	1	x	x	0	0	0	0	0	Select unit ØØ to begin activating input cards. Input card timing circuits enabled by ISL = 1, computer program would ignore handshake flag (TME = 0), which must be returned when activating cards.
Address	0	0	0	0				Not used									Activate input card slot ØØ, unit ØØ. Computer gate must be issued. Input card starts to time out.
Address	0	0	0	1				Not used									Activate input card slot Ø1, unit ØØ.
								⋮									⋮
																	Activate all desired input cards in unit ØØ.
																	⋮
								IEN ISL				TME					
Control	1	1	1	1	x	x	x	0	1	x	x	0	0	0	0	1	Select unit Ø1 to activate its input cards.

Table 3-2. Typical Interrupt Search Input Mode Programming Sequence (Continued)

TYPE WORD	PROGRAMMED WORD																FUNCTION
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Address	0	0	0	0	Not used												Activate input card slot ØØ, unit Ø1.
																	Activate all desired input cards in system.
					2. Enable Interrupt												
								IEN	ISL			TME					
Control	1	1	1	1	x	x	x	1	x	0	x	1	x	x	x	x	Enable interrupt mode by IEN = 1 and wait for first activated input card to signal ready with the common flag line, TME = 1.
					Assume an input card goes ready.												
					3. Turn off interrupt enable mode.												
Control	1	1	1	1	x	x	x	0	1	x	x	0	0	0	0	0	Select unit ØØ to begin searching for ready input card. Turn interrupt mode off by IEN=0; turn on input mode by ISL=1; turn off TME to generate handshake flag (TME=0).
					4. Begin input card search												
Address	0	0	0	0	Not used												Search slot ØØ, unit ØØ for ready data. Card data displayed in switch register bits 0-11. RETURN DATA lamp displays input request status (IRQ).
																	Input card search can be in any order.
Address	1	1	1	0	Not used												Search last slot, unit ØØ for ready data.
Control	1	1	1	1	x	x	x	0	1	x	x	0	0	0	0	1	Select unit Ø1 for input card ready search.
Address	0	1	0	1	Not used												Search all activated cards in any order to determine ready card. Card slot 5 arbitrarily assumed to be ready, RETURN DATA lamp on.
Address	0	1	0	1	Not used												Reactivate card slot 5, unit Ø1 for next input data.
								IEN	ISL			TME					
Control	1	1	1	1	x	x	x	1	0	0	x	1	x	x	x	x	Turn on interrupt enable mode again and wait for next input card to to signal ready.

Table 3-3. Typical Dedicated Input Programming Sequence

TYPE WORD	PROGRAMMED WORD																FUNCTION
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Control	1	1	1	1	x	x	x	0	1	0	x	1	0	0	0	0	Select unit ØØ for input mode.
Address	0	0	0	0	Not used												Activate input card ØØ, unit ØØ with computer gate. Wait for card to signal ready with timing flag.
	Assume card signals ready; card data displayed in switch register bits 0-11.																
Address	0	0	0	0	Not used												Reactivate card with address word and computer gate (ISL still on).
	All data received; deactivate card.																
Control	1	1	1	1	x	x	x	0	0	0	x	0	0	0	0	0	Select unit ØØ with ISL off.
Address	0	0	0	0	Not used												Address card ØØ, unit ØØ with computer gate.

for any of the following conditions:

a. Power failure.
b. Setting LINE switch to OFF.
c. Removal of data input plug P1.
d. Programming bit 5 = 0.
e. Removal of mainframe card A3.
f. Crowbar circuit activiated.

3-164 Power Supply Crowbar

3-165 The main +5 volt power supply has a built-in crowbar feature to protect the mainframe circuits and the output cards from damage due to excessively high power supply voltages. The crowbar circuit monitors the +5 volt line and energizes an SCR crowbar if the monitored voltage rises above +6.2V volts. Once energized, the crowbar circuit forces the +5 volt supply into current latch, reducing the power supply voltage to approximately +0.7 volts. The indicator on logic and timing card A3 will turn off if the power supply crowbars. The crowbar circuit can be reset by first eliminating the cause of the overvoltage condition and then setting the LINE switch OFF and ON.

NOTE

If the cause of the overvoltage condition is a short circuit between the +12 volt line and the +5 volt line, the crowbar circuit will also blow fuse F2, which interrupts the +5V and +12V power supply outputs.

3-166 Current Latch

3-167 The current latch circuit monitors the main +5 volt power supply current. If the current exceeds 6.5 amperes, the +5 volt power supply will go into the current-latch condition. This reduces the +5 volt output to less than 1 volt. The supply will remain in this state until the LINE switch is switched OFF, the overload condition is removed, and S1 is switched ON. While in current latch, all front-panel LEDs remain off.

NOTE

When resetting latch circuit, wait at least 10 seconds before turning unit back on.

SECTION IV
PRINCIPLES OF OPERATION

4-1 INTRODUCTION

4-2 This section contains principles of operation for the 6940B Multiprogrammer. The section is divided into three main paragraphs: First, a basic block diagram discussion; second, a detailed block diagram discussion covering all logic circuit operations and finally, a detailed analysis of the electronic circuits not covered in the logic discussion.

4-3 BASIC BLOCK DIAGRAM DISCUSSION

4-4 Figure 4-1 is an overall block diagram of the 6940B showing the four major circuits of the 6940B together with the principal input and output signals of each circuit. Each major circuit has an associated sheet number for correlation of this diagram with the four schematic sheets at the rear of the manual. It should be noted that the logic circuits and signal designations shown in Figures 4-1 and 4-4 represent simplified logical operations. The actual circuit implementation of these functions is covered in the detailed block diagram discussion.

4-5 The 6940B is the master control and data distribution unit for bidirectional Multiprogrammer Systems. Although the 6940B operates bidirectionally, the first programming steps are always in the output direction to initialize the Multiprogrammer System and to establish operating modes.

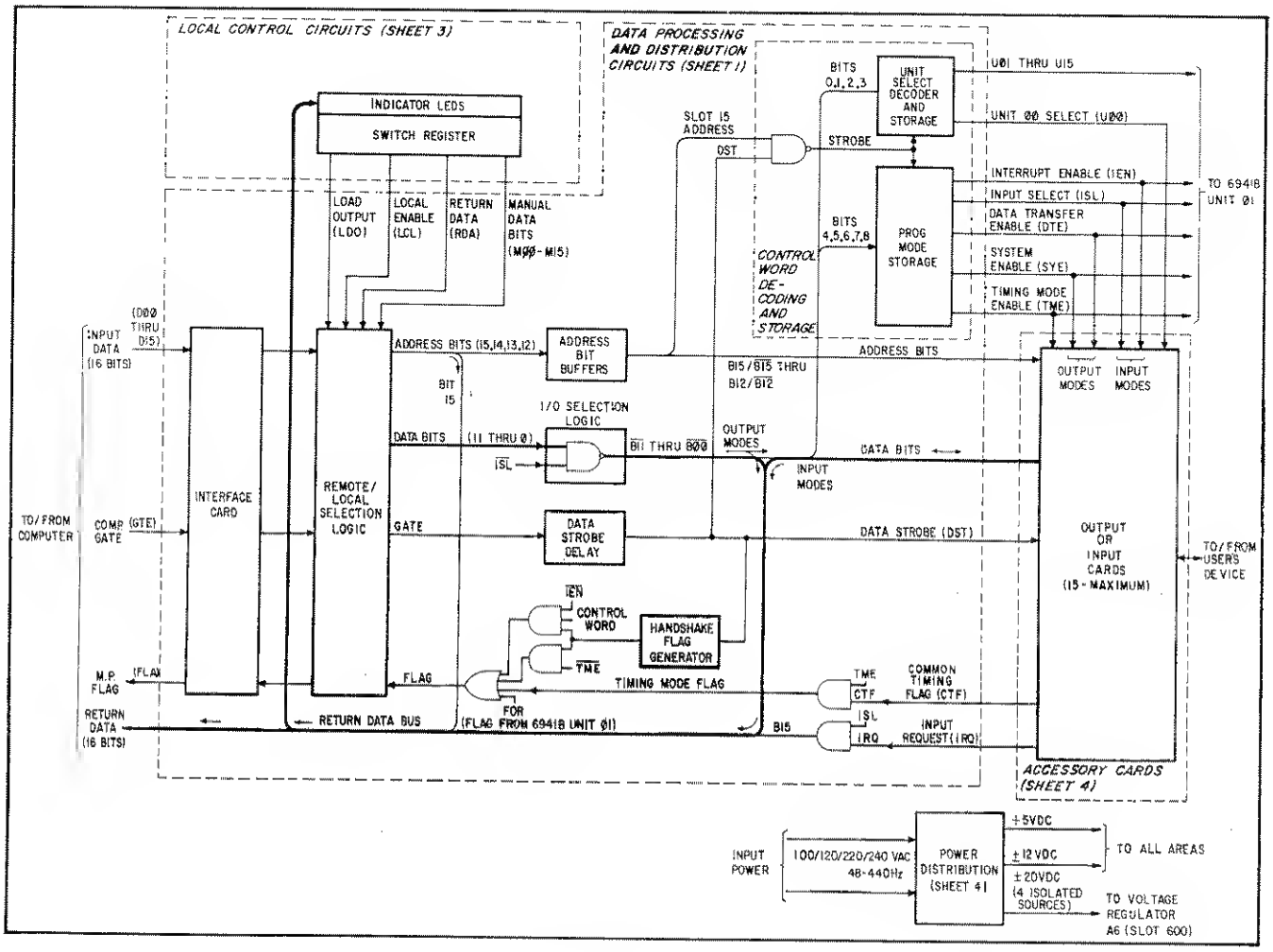


Figure 4-1. Basic Block Diagram

4-6 Computer data is received in the form of 16-bit parallel words and applied to the interface card of the 6940B. The interface card provides the proper termination for the computer output circuits. The data-bit outputs of the interface card, together with a set of manually selected data from the local switch register are applied to the remote/local selection logic circuits. When LOCAL operation is selected, a local enable line (LCL) blocks the path for computer data and gates through the manually programmed data. When REMOTE operation is selected, the computer data is gated-through and local data is blocked. The 16-bits selected by the remote/local circuits are divided into two groups; address bits (bits 15, 14, 13, and 12) and data bits (bits 11 through 0). The four address bits are applied to a set of buffer amplifiers which produce the true and complemented forms (B15/$\overline{B15}$ through B12/$\overline{B12}$) of the address bits. Simultaneously, the 12-data bits are gated through I/O selection logic (since no modes have yet been programmed).

After an 8μsec software delay which allows the input data lines to settle, the computer issues a gate signal. The computer gate signal is interfaced and selected as described for the input data bits and applied to a data strobe delay circuit. Prior to the gate being issued by the computer, the multiprogrammer is in a "wait" condition; the address and data bits are distributed to the 400 series accessory card slots and to the control word decoding and storage circuits, but do nothing while awaiting a data strobe. When the computer gate appears, the data strobe delay circuit waits 2μsec and then generates a data strobe signal. Assuming the computer input to be a control word (as it must be for the first programming step) address bits 15, 14, 13, and 12 will all be binary 1's, signifying slot address 15. Slot address 15, combined with DST, strobes bits 0 through 3 into unit select storage registers and bits 4 through 8 into mode storage registers. Bits 0, 1, 2, and 3 are decoded by the unit select logic and energize one of 16 unit select lines (U00 through U15) according to the programmed address. The energized unit select line partially enables all 15 accessory card slots of the selected unit. The unit selection is stored and will remain in effect until a new unit is address by a later control word.

4-7 From this point in operation the 6940B will either function as an output device, supplying programmed data to selected output cards; or as an input device, reading digital data from selected input cards and returning this data to the computer. The output-input status depends on the programmed state of the input select (ISL) mode bit.

4-8 Output Modes

4-9 In the absence of an input mode selection the 6940B will function as an output device. Two of the five programmable modes, SYE and DTE, relate exclusively to output functions; TME is used for both output and input modes. Each of these three functions is covered briefly in the following paragraphs.

4-10 **System Enable Mode.** The system enable mode (SYE) is selected when bit 5 of a control word is programmed to the 1-state. SYE is routed from the programmed mode storage circuits to all accessory card slots in the system. Prior to SYE being programmed, the output circuits of all output cards are disabled; resistance outputs are short circuited, voltage outputs are held at 0 volts, current outputs are opened, relay contact outputs are held open, and TTL outputs are at logical Ø's. When SYE is programmed, the output cards are allowed to respond to programmed data. SYE is reset by programming bit 5 = 0, by removing power, or by removing card A3. As an added safety feature, a jumper on input data plug P1 completes the SYE path to all card slots, making it necessary to have input computer data connected in order to enable the output cards in the system.

4-11 **Timing Mode.** The timing mode (TME) is utilized for both output and input operations. It is selected by programming bit 4 of a control word to the 1-state. For output functions, TME causes the flag signal returned to the computer to be held in the busy state until the programmed output cards have completed processing their last data input. The busy state of the flag signals the computer not to input new data. TME is distributed to all timing mode flag circuits of all units in the system. The mode remains in effect until programmed out of the mode by bit 4 = 0.

4-12 **Data Transfer Enable Mode.** The data transfer enable mode (DTE) is selected by programming bit 6 = 1. DTE is wired to all accessory card slots of the system but is utilized only by output cards having dual-rank storage, by relay output cards and by TTL output cards. Output cards with dual-rank storage have two sets of storage registers. The first set of registers store the programmed data as it is strobed in by DST. The second set of registers receive the data from the first set of registers and apply it to the output conversion circuits only when DTE is programmed.

4-13 For output cards with dual-rank storage, the DTE mode is normally used in either of two ways:

(1) *DTE is selected first and latched.* The output cards are then addressed and programmed one at a time. Since DTE is present, the programmed data is transferred immediately from the first set of registers to the second set of

registers to the conversion circuits. Each card thus produces an output proportional to the programmed data, as it receives the data.

(2) *DTE is not initially selected.* The output cards are addressed and store the programmed data in the first set of registers, but do not transfer the data to the second set of registers, since DTE has not been programmed. This method permits the first registers of all cards of this type to be loaded with data first; then by programming DTE, the outputs of all the cards are simultaneously transferred to the user's system. The output cards will continue to hold the most recently programmed value after DTE is removed.

4-14 The digital (TTL) and relay output cards have only a single level of storage and the output relays respond to data as the card is programmed. However, a gate line (or a contact closure available on each relay output card) is enabled only when DTE is programmed. The gate line (or contacts) can be used in the external system to initiate two operations:

(1) To simultaneously strobe the outputs of all digital and/or relay output cards into the external system.

(2) To start a timing flag circuit in the external system that will hold the flag line returned to the multiprogrammer in the busy state until the circuit times out. The delay provided by this circuit should coincide with the maximum time required for the user's system to process the digital or data relay outputs.

4-15 **Computer Data Input.** For output modes, the output cards are programmed by 16-bit data words from the computer. A data word contains two types of information; slot address (bits 15, 14, 13, and 12 programmed to any number from 0000 to 1110) and data (bits 11 through 0). A unique combination of the four address bits is wired to each of the 15 card slots. Slot 400 receives address 0000; slot 401 receives 0001; . . . slot 414 receives 1110.

4-16 The same slot address wiring is carried through in all units so that when a given slot address is programmed, all slots in the system having that address are partially enabled. However, only one unit of the system can be selected at a time, so only the slot of the unit selected by a previous control word is fully enabled to accept the data contained in bits 11 through 0. (Input-type cards require ISL in addition to the appropriate slot and unit addresses to be enabled.) The 6940B Multiprogrammer is assigned unit number 00 (U00), while the extender units are numbered consecutively from U01 up to U15.

4-17 **Handshake Mode.** Computer data is entered into the multiprogrammer in either of two modes; the handshake mode or the timing mode. The return path to the computer for the handshake flag is enabled when TME is programmed off, and blocked when it is programmed on. An alternate path for the handshake flag is enabled when a control word is programmed, provided IEN (interrupt enable) is not being selected by that control word. For output modes, it can be assumed that IEN will always be off and the alternate path will be enabled for all control words, even if TME is on. The significance of the alternate path for control words will be covered in detail in the description of input modes, Paragraph 4-21.

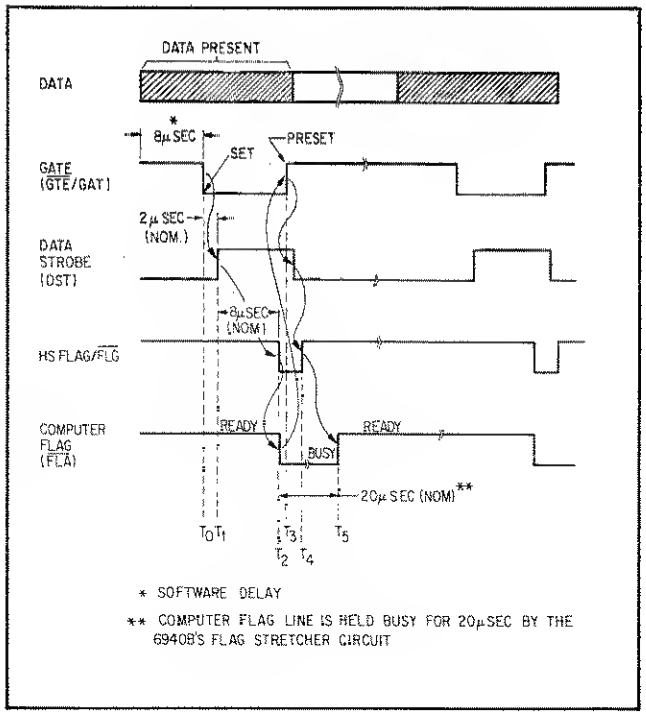


Figure 4-2. Handshake Mode, Timing Diagram

4-18 In the handshake mode, the multiprogrammer will accept data at rates up to 20k words/sec. A timing diagram of the data, gate, flag and data strobe signals for the handshake mode are given in Figure 4-2. The significant multiprogrammer and computer operations at each time interval are described as follows:

NOTE

Because the multiprogrammer system is designed to operate with up to 100 feet of cabling between each unit, in 8μsec software delay is required between data output to the multiprogrammer and setting the gate signal (see Section III).

T_0 – Following the 8μsec software delay, the gate signal from computer goes LO indicating that a word is available on the 16 data input lines. The gate signal is applied to a data strobe delay circuit in the 6940B, and to identical cir-

cuits in all extender units in the system.

T_1 – Following a 2μsec delay, the data strobe delay circuit switches DST to a HI level. This level loads the programmed data into the control word decoding logic (if a control word code is present) or into an addressed output card.

T_2 – After a delay of approximately 8μsec from the start of the gate, the handshake flag generator sets the handshake (H.S.) flag LO which is applied to a flag stretcher circuit in the 6940B setting the flag line ($\overline{FLA}$) back to the computer LO (busy). This indicates to the computer that the data input operation has been completed. The computer must reset the gate at this time. Data may be removed after the gate is reset.

T_3 – The gate line is reset (goes HI) in preparation for the next data output operation.

T_4 – When the gate line is reset, the data strobe delay circuit resets DST and the handshake generator resets the H.S. flag ($\overline{FLG}$ goes HI) allowing the computer flag ($\overline{FLA}$) to go HI. Note that the 6940B's flag stretcher circuit (see paragraph 4-49) holds the $\overline{FLA}$ signal LO (busy) for 20μsec.

T_5 – The computer flag ($\overline{FLA}$) goes HI (ready). The computer may initiate a new data output cycle anytime after T_5.

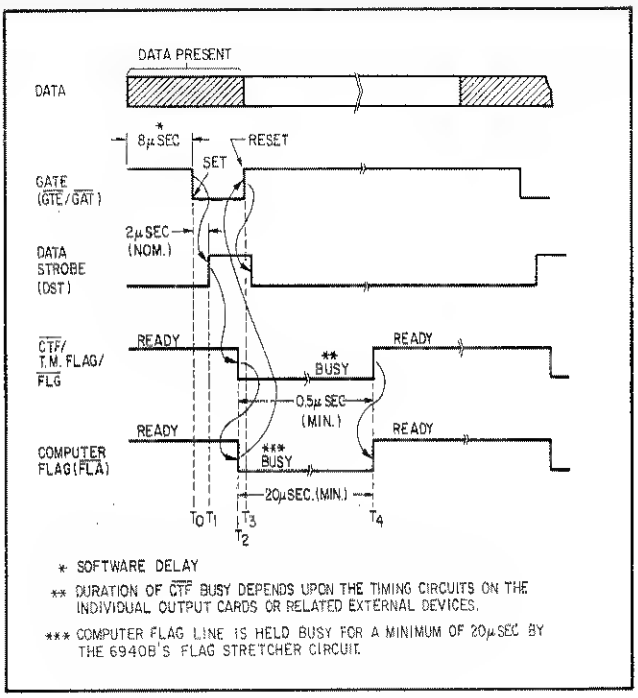


Figure 4-3. Timing Mode, Timing Diagram

4-19 **Timing Mode.** Whenever an output card is addressed and data is strobed in, a CTF pulse is produced by a timing circuit on the addressed card or a timing circuit on the device attached to the addressed card. This flag pulse (Figure 4-3) is initiated by DST but its duration depends on the timing circuit on the individual output cards or related external device. The timing flag duration for a particular output card is selected on the basis of the maximum time required for the card, or the external device connected to it, to complete processing data before it can accept new data. The timing flag output of the individual cards are ORed together to become the common timing flag (CTF). When the timing mode is not programmed, CTF is still generated by the output cards but has no effect on the flag line back to the computer. When TME is programmed, the CTF pulse becomes the flag to the computer. In the timing mode, the flag is held busy until the timing flag pulses from the individual output cards have timed out. The flag stretcher circuit in the 6940B holds the computer flag ($\overline{FLA}$) line busy for a minimum of 20μsec.

4-20 Extender Unit Flags. Every extender unit in the system has a flag circuit similar to the 6940B flag circuit. Figure 4-4 is a block diagram showing the interconnection between flag circuits. As can be seen from Figure 4-4, a handshake or timing flag generated by an extender unit is ORed through each unit in the system to the 6940B master unit. The 6940B receives the flag line as FOR and returns it to the computer (via the flag stretcher circuit) as the system flag. The operation of the extender unit flag circuits is identical to the master unit flag circuit.

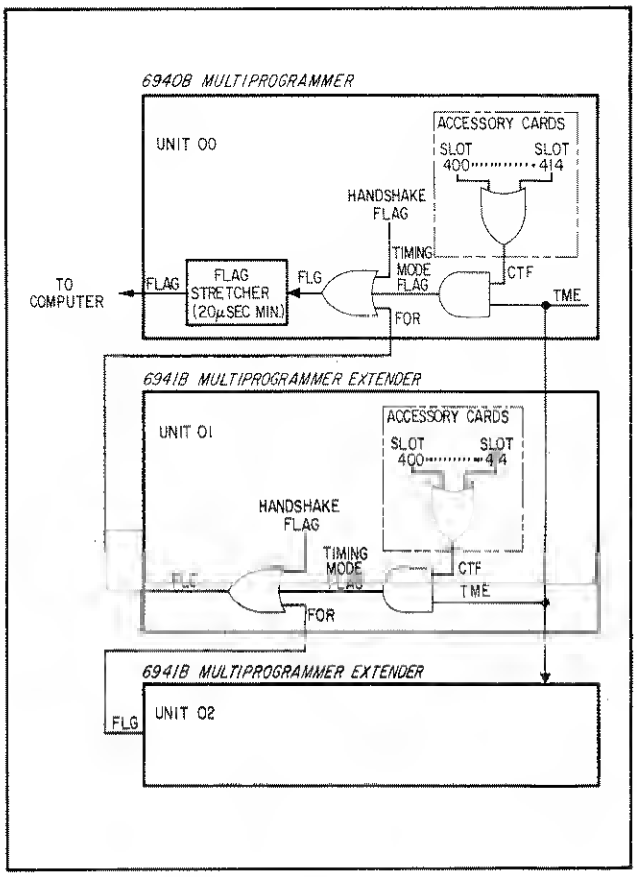


Figure 4-4. Flag ORing Circuits, Block Diagram

4-21 Input Modes

4-22 As described in Section III, there are two primary input modes and a number of secondary variations of these modes involving both hardware and software options. The two primary modes are designated:

(1) The Dedicated Input Mode
(2) The Interrupt Search Mode.

4-23 The basic theory of operation for input functions will be described in terms of the two primary input modes as related to a typical digital input card.

4-24 **Dedicated Input Mode.** In this mode, the computer reads data from input cards on an individual card basis. Until it completes its operation on the currently addressed card, the computer should not go on to another input card. The dedicated input mode is normally used in either of two ways; ungated, or in the timing mode.

4-25 *Ungated.* This is the most basic method of reading data from an input card. The procedure is accomplished in two programming steps: (1), programming a control word with ISL = 1, IEN = 0, and TME = 0; and (2), programming the desired card address and *not* issuing a computer gate signal.

NOTE

Because the multiprogrammer system is designed to operate with up to 100 feet of cabling between each unit, a software delay must be incorporated between addressing an input card and reading its data without a gate. Refer to paragraph 3-133.

4-26 In Step (1), ISL = 1 simply turns the 12-data bit lines of the multiprogrammer in the direction of the computer. Although ISL is also applied to the input cards it has no effect on their operation in the ungated mode.

4-27 In Step (2), the 12-data bits currently stored on the addressed input card are placed on the return data lines and will remain there for as long as the card address is present. Since a computer gate is not issued in this mode, the multiprogrammer does not produce a data strobe (DST) and the addressed card is not armed. (CTF and IRQ are neither generated nor required in the ungated mode.)

4-28 *Timing Mode.* This mode is also programmed in two steps: (1), a control word is programmed with ISL=1, IEN= 0, and TME = 1; and (2), the desired card address is issued along with a computer gate signal.

4-29 Step (1) sets up three initial conditions for this mode: First, ISL reverses the direction of the 12 data bit lines; second, ISL is applied to all input cards as a condition necessary to enable (arm) an input card when it is addressed and data strobed; and third, TME enables the common timing flag (CTF) return path from the input cards to the computer.

4-30 In Step (2), the address of the desired input card is programmed along with a computer gate. Upon receipt of its address bits, the selected input card will immediately place 12-bits of data on the return data bus to the computer. However, the computer should not accept this data until the multiprogrammer signals, via the trailing edge of CTF, that the input data from the addressed card has been updated and is now ready to be read.

4-31 Within the selected input card, the combination of ISL, DST, and the card address will send a gate signal to the external device and simultaneously reset the flag flip-flop on the input card. Resetting the flag causes the CTF line back to the multiprogrammer to switch to the busy state. When the external device is ready with new data it will signal the input card via the trailing edge of its device flag. This edge will set the input card flag flip-flop which will return the CTF line to the ready state. At the same time, new data will be strobed into the storage registers on the input card. The computer should interpret the trailing edge of CTF as permission to read the return data.

4-32 Before going on to an interrupt-search mode, previously armed cards whose flag flip-flops have been set should either be rearmed (by programming ADDR·DST·ISL) or disarmed (by programming ADDR·DST·$\overline{\text{ISL}}$), with either operation done in the handshake mode.

4-33 **Interrupt-Search Mode.** The interrupt-search mode offers an efficient means of retrieving data from groups of input cards. As covered in Section III of this manual, there is a hardware option available which adds versatility to this mode by allowing all digital input cards with jumper W6 installed to be armed as a group. However, in order to keep this explanation simple, the multiprogrammer operation in the interrupt-search mode will be described in terms of four basic programming steps, with W6 *not* installed. (Figure 3-12A is a timing diagram of the interrupt-search mode.)

Step 1. Establish initial mode conditions by programming a control word with ISL = 1, IEN = 0, and TME = 0.

Step 2. Arm desired input cards by programming card addresses. (A computer gate must accompany each address as it is programmed.)

Step 3. Select the interrupt enable mode by programming a control word with IEN = 1, TME = 1, and ISL = X (X = doesn't care).

Step 4. Wait for the multiprogrammer CTF flag to indicate that one or more addressed input cards has valid data ready. Then, poll the input cards (by issuing their addresses)

in a software determined order. Do not issue a computer gate while polling. A programmed delay (wait time) must be incorporated between addressing each input card and reading its data without a gate. The delay time depends upon the multiprogrammer unit number (0-15) of the addressed card (see paragraph 3-133). Examine bit 15 of each return data word in the computer and accept the data only when bit 15 = 1. (The state of bit 15 is determined by IRQ from the addressed input card; when the addressed input card has valid data available, IRO makes bit 15 = 1.)

4-34 Step (1) establishes two initial conditions for this mode: First, ISL reverses the direction of the 12 data bit lines; and second, ISL is applied to all input cards as a condition necessary to enable (arm) an input card when it is addressed and data strobed. Since the timing mode has been programmed off in this step, subsequent data transfers between the computer and the multiprogrammer will be done in the handshake mode.

4-35 In Step (2), the address of the desired input card is programmed along with a computer gate. Upon receipt of its address bits, the selected input card will momentarily place 12-bits of data on the return data bus to the computer. The computer should ignore this data.

4-36 As in the dedicated input timing mode, the combination of ISL and DST and the card address arm the addressed card; a gate is sent to the external device and the flag flip-flop on the card is reset. When the device is ready with new data it will signal the input card via the trailing edge of its device flag. This edge will set the flag flip-flop and strobe new data into the storage registers on the input card. When the interrupt mode is programmed in the next step, the "set" flag flip-flop on this, or any other input card with new data ready, will generate an interrupt. Also, when the input cards are polled in the search mode, any card whose flag flip-flop is set will cause IRO, and thus bit 15 returned to the computer, to be true.

4-37 Step (3) establishes conditions for enabling interrupts from previously armed input cards which now have data available. Along with the control word containing IEN = 1 and TME = 1, the computer must also issue a gate signal. When the control word containing IEN = 1 is programmed, a handshake flag is not generated. The computer should now wait for a transition of the CTF line from an input card to signal an interrupt. Within the input cards, IEN and DST (derived from the computer gate) are logically ANDed with the output of the flag flip-flop, which is true when the external device has data ready. When all three conditions are true on any input card, the CTF line will be set to the busy state. This transition of the CTF line to the busy state signals the computer to reset its gate, which in turn resets DST. With DST reset, the CTF AND-gate within the input cards is inhibited, causing CTF to return to the ready state. The computer interprets this transition as an interrupt request.

4-38 In Step (4), the address of each input card of the selected group is programmed in a program assigned order, without a computer gate. As each card is addressed, it places its 12-data bits on the return data bus. The card address is also ANDed with the output of the flag flip-flop on the input card, and when both are true (signifying that the addressed input card has new data) the IRQ signal is made true. IRO directly controls the state of bit 15 returned to the computer; when bit 15 is true, the computer should accept the associated 12 data bits.

4-39 DETAILED BLOCK DIAGRAM DESCRIPTION

4-40 Figure 7-1 is a detailed block diagram of the 6940B Multiprogrammer showing all logic operations carried out by the unit. Detailed electronic circuits are represented by function blocks on this diagram but are also described fully under detailed circuit analysis using the schematic diagrams.

4-41 Logic Definitions

4-42 The internal logic circuits of the 6940B are designed within and conform to the definition of positive logic. This simply means that a logical 1 is represented by a voltage level more positive than a logical 0 and that the basic logic elements (AND gates, NAND gates, and flip-flops) are utilized within this framework. The actual logic levels utilized within the multiprogrammer are:

LOGIC 1 = +2.4V to +5.5V (HI)
LOGIC 0 = 0V to +0.4V (LO)

4-43 A system of mnemonics is also used to identify functions implemented at specific points throughout the system. Mnemonics are three character abbreviations of the signal function name. A signal function may be designated in either its true form (e.g., LCL) or its complemented form ($\overline{\text{LCL}}$). When a particular function is set to its assertive state, its true form = logical 1 (HI) and its complement = logical 0 (LO). The opposite states exist when the function is not asserted. A few examples will be given relative to this system to expand on the previous definitions:

(1) When the DATA SOURCE switch on the switch register is set to the LOCAL position, the LCL and $\overline{\text{LCL}}$ signal lines assume the following states:

LCL = 1 (HI) $\overline{\text{LCL}}$ = 0 (LO)

(2) When a flag signal is generated by the logic and timing card, the $\overline{\text{FLG}}$ line makes a transition from a logical 1 (HI) to a logical 0 (LO) and returns to a logical 1 (HI) when the flag has been completed.

(3) When a specific bit is programmed to a logical 1 at the computer, the corresponding $\overline{\text{D}}$—— input line to the mul-

tiprogrammer goes to the logical 0 (LO) state. Thus, the D-- designations on the input lines specify negative-true levels.

4-44 Input Card A1

4-45 The 16 data bits ($\overline{D15}$ through $\overline{D00}$) and a gate signal ($\overline{GTE}$) from the computer are applied to identical termination networks on input card A1. The networks minimize noise and ringing on the transmission lines by providing the ideal line termination impedance. The 1kΩ pull-up resistor in the $\overline{FLA}$ return circuit improves the 1-state driving capability of the output NAND gate (G35) on the remote/local card.

4-46 Remote/Local Card A2

4-47 **Data Selection.** Data bits $\overline{D15}$ through $\overline{D00}$ are applied to input NAND gates G15 through G0 and gate signal $\overline{GTE}$ is applied to gate G32. The second input to each NAND gate is $\overline{LCL}$ from the local switch register. If LOCAL operation *is not* selected, $\overline{LCL}$ = 1 (HI) and the NAND gate outputs are allowed to follow (but invert) the computer input data. If LOCAL operation *is* selected, $\overline{LCL}$ = 0 (LO) and the NAND gate outputs are held at a constant HI level.

4-48 Output NAND gates G31 through G16 receive manual data bits M15 through M00 from the switch register as one input, and the output of gates G15 through G0 as the other input. In REMOTE operation, M15 through M00 are all held in the HI-state allowing the output NAND gates to pass the computer data to the rest of the system. In LOCAL operation, the manual data bits assume the states selected by the switch register programming switches, and since $\overline{LCL}$ (through the input NAND gates) holds the second input to G31 through G16 in the HI-state, the manual data bits are passed to the system.

4-49 Computer gate signal $\overline{GTE}$ or switch register gate LDO is selected as the multiprogrammer gate ($\overline{GAT}$) by gates G32 and G33. Either $\overline{FLG}$ from logic and timing card A3 or RDA from the switch register is selected by gates G34 and G35 and returned to the computer as the system flag ($\overline{FLA}$). One-shot multivibrator Z13 produces a 20μsec positive output pulse on receiving a positive-going transition at its input. Transistors Q1 and Q2 act as an OR gate, combining Z13's input and output signals to maintain a minimum duration of 20μsec for the system flag ($\overline{FLA}$) signal to the computer.

4-50 Selected data bits $\overline{B15}$ through $\overline{B00}$ are routed in various combinations to logic and timing card A3; to switch register A11; and to the return data bus off the back-plane wiring, as described below:

(1) Address bits $\overline{B15}$ through $\overline{B12}$ are routed through cable W1 to LED drivers in switch register A11 to provide a visual indication of the programmed address.

(2) Data bits $\overline{B11}$ through $\overline{B00}$ are routed through cable W2 to logic and timing card A3. If an input mode has *not* been programmed, the computer generated data bits are buffered on card A3 and looped-back through the back-plane wiring to remote/local card A2. If an input mode has been programmed, $\overline{B11}$ through $\overline{B00}$ become the input data bits from an addressed input card. In either case, $\overline{B11}$ through $\overline{B00}$ will be returned to the computer through the return data bus and jumpered through card A2, into cable W1, and then to the switch register. For output modes, switch register LEDs 11 through 0 will display the status of the programmed data bits; for input modes, the same LEDs will display the status of data bits returned by an addressed input card.

(3) Address bits $\overline{B14}$, $\overline{B13}$, and $\overline{B12}$ are buffered and coupled through the back-plane to logic and timing card A3.

4-51 **IRQ Logic.** The IRQ logic circuits control the state of bit $\overline{B15}$ returned to the computer as a function of the operating mode (output or input) and the state of $\overline{IRQ}$.

4-52 For output modes, $\overline{B15}$ from the computer is simply passed through gates G37 and G38 (because of ISL being off) and returned to the computer as $\overline{B15}$ in the same logic state as it was received.

4-53 For input modes, the state of $\overline{B15}$ will reflect the state of $\overline{IRQ}$ from the input cards. When $\overline{IRQ}$ is true (LO), meaning that the data returned from the currently addressed input card is valid, $\overline{B15}$ will also be made true (LO) by the IRQ logic gates. When the computer examines the return data word and finds $\overline{B15}$ true, it will accept the 12 data bits of that word; if it finds $\overline{B15}$ false, it will reject the 12 data bits.

4-54 $\overline{IRQ}$ is logically NANDed with ISL by gate G39. If ISL has been programmed on, the output of G39 will follow, but invert, whatever state $\overline{IRQ}$ happens to be. If $\overline{IRQ}$ is LO, the HI output of G39 will be NANDed with the HI output of G37. The resulting LO output of G38 (the true state of $\overline{B15}$) is buffered by non-inverting amplifier Z12 before being returned to the computer.

4-55 **Local FLAG Logic.** The local FLAG logic effectively "wire-ORs" $\overline{FLA}$ and $\overline{IRQ}$. When an output mode is in effect, $\overline{FLA}$ is passed by gates G41 and G42 and routed through cable W1 to the RETURN DATA LED driver on switch register A11. For input modes, $\overline{IRQ}$ is passed by G40 and replaces $\overline{FLA}$. Thus, for output modes, the RETURN DATA LED indicates the status of the flag return line to the computer while for input modes it indicates the status of IRQ.

4-56 Logic and Timing Card A3

4-57 Logic and timing card A3 performs data and address bit buffering, I/O data bit selection, and data strobe and flag signal generation.

4-58 **Address Bit Buffers.** This circuit group consists of four two-stage inverting amplifiers. An output is taken from both the first and second inverter stages, thus producing the true and complemented forms of the input address. This operation is necessary in order to develop 16 unique combinations of 4 slot address bits for distribution to each of the 15 card slots and to the control word gate in unit select card A5.

4-59 **I/O Selection.** Input data bits $\overline{B11}$ through $\overline{B\emptyset\emptyset}$ from the remote/local card are amplified and inverted by Z2 and Z1 and applied to I/O selection gates G11 through G$\emptyset\emptyset$. If the input select mode *has not* been programmed ($\overline{ISL}$, HI), the I/O selection gates will pass the programmed data bits to the 15 accessory card slots. If the input select mode has been programmed ($\overline{ISL}$, LO) gates G11 through G$\emptyset\emptyset$ will be inhibited. Under these conditions, B11 through $\overline{B\emptyset\emptyset}$ will represent data returned from an addressed input card.

4-60 **Data Strobe Generation.** The data strobe signal is derived from the computer GATE input. For output modes, DST serves to strobe data into storage registers on addressed output cards. For input modes, DST is involved in gate-flag functions on the input cards (see Paragraph 4-98).

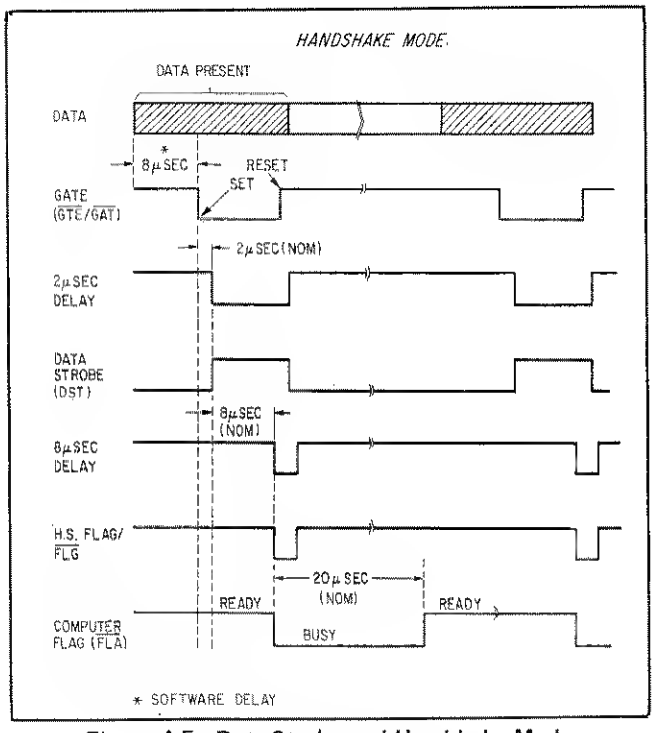


Figure 4-5. Data Strobe and Handshake Mode, Timing Diagram

4-61 A timing diagram showing the relationship between the GATE input and DST is given in Figure 4-5. On program command, the computer will set the GATE input line, and thus $\overline{GAT}$ to the LO state. The output of the 2μsec delay circuit is held in the LO state until the 2μsec delay has expired, at which time it goes HI. The signal is amplified by the DST amplifier and then transferred to the rest of the system. DST will remain HI until $\overline{GAT}$ is reset. At that time, both the output of the 2μsec delay circuit and DST are reset.

4-62 Handshake Flag Generation. The handshake flag is generated and returned to the computer for either of two sets of conditions:

(1) Whenever the computer issues a gate signal and the timing mode is off (TME = 0). This is the standard handshake mode and pertains to all control, data, and address word transfers.

(2) A handshake flag is generated when a control word is being programmed with TME on (TME = 1), interrupt enable mode off (IEN = 0), and no output cards are currently timing out ($\overline{CTF}$ is HI). If an output card is in the process of timing out ($\overline{CTF}$ is LO) when this control word is being programmed, the computer flag line will be held BUSY until the card times out.

4-63 When a control word is being programmed with IEN on (IEN = 1), the handshake flag is inhibited. The handshake flag is inhibited because, with the interrupt enable mode on, it is necessary that the input cards determine the state of the flag returned to the computer. Paragraph 4-103 covers this function in detail.

4-64 As shown in Figure 4-5, the normal handshake flag, like DST, is derived from the input $\overline{GAT}$ signal. It is started 10μsec after the $\overline{GAT}$ line goes LO, and terminates shortly after $\overline{GAT}$ goes HI. The output of the 2μsec delay circuit is used to trigger an 8μsec delay circuit. At 10μsec after $\overline{GAT}$ initially goes LO, the input to NAND gate G12 from the 8μsec delay circuit goes HI. This HI level is NANDed with U$\emptyset\emptyset$ (HI if unit 0 has been selected) and the output of gate G15 (HI if the timing mode is off, TME = 0). The resulting LO output of gate G12 is propagated through flag OR gates G13 and G14 to become $\overline{FLG}$. The $\overline{FLG}$ signal is applied to gates and the flag stretcher circuit on board A2. These circuits produce a LO level (BUSY) $\overline{FLA}$ signal when $\overline{FLG}$ is received. The transition of $\overline{FLA}$ to the LO (BUSY) state indicates to the computer that the multiprogrammer has completed storage of the programmed data. Following a short delay, the computer sets the $\overline{GAT}$ line HI. The output of the 2μsec and 8μsec delay circuits follow the $\overline{GAT}$ signal, returning the $\overline{FLG}$ output to the HI state. With $\overline{FLG}$ HI, the flag signal ($\overline{FLA}$) to the computer is allowed to go HI. The flag stretcher circuit on board A2 holds the $\overline{FLA}$ signal LO (BUSY) for a minimum of 20μsec as shown on Figure 4-5.

4-65 The alternate handshake flag is generated in a manner similar to that described above. The main difference is that when a control word (with TME on and IEN off) is programmed, a circuit on the unit select card generates a $\overline{CTF}$ signal which is time coincident with the output of the 8μsec delay circuit on the logic and timing card, and this signal controls gate G15. $\overline{CTF}$ is inverted by G15, and together with U00 and the HI output of the 8μsec delay circuit enables gate G12.

4-66 **Timing Mode Flag Generation.** Whenever the timing mode is in effect (TME = 1) the flag signal returned to the computer will be controlled by the $\overline{CTF}$ signal from the accessory cards. Gate G17 implements the simple NAND function $\overline{TME \cdot CTF}$ and passes the resulting timing mode flag through flag OR gates G13, G14 and boards A2, A1 to the computer.

4-67 For output modes, $\overline{CTF}$ goes LO at the time data is strobed into an addressed output card and stays LO (busy) until a timing circuit on the output card, or the external device associated with output card, times out. The leading edge of $\overline{CTF}$ indicates to the computer that the multiprogrammer has stored the programmed data and that the computer can reset the gate and remove the data. The trailing edge of $\overline{CTF}$ tells the computer that the last set of programmed output data has been processed and that new data can be sent to the output cards.

4-68 For input modes, the leading edge of $\overline{CTF}$ notifies the computer to reset the gate and remove its last input. When IEN is programmed, the trailing edge of $\overline{CTF}$ represents an interrupt request to the computer.

4-69 Unit Select Card A5

4-70 Unit select card A5 examines the states of address bits B15, B14, B13, and B12, and if they are all HI's (indicating the presence of a control word) it strobes the states of $\overline{B00}$ through $\overline{B08}$ into local storage registers.

4-71 **Control Word Gate.** Control word NAND gate G1 receives address bits B15, B14, B13, and B12. If slot address 15 is programmed (indicating a control word) the output of G1 goes LO, is inverted, and applied to NAND gate G3 together with DST. When DST appears, the resulting LO output of G3 is inverted by Q2 and applied to the clock (CLK) inputs of the control bit and unit select storage registers.

4-72 **Control Bit Storage.** The control bit storage registers are D-type positive-edge triggered flip-flops with direct preset capability. The logical state at the D-input terminal is transferred to the O-output terminal whenever the common clock (CLK) input is strobed by a positive going pulse. ($\overline{O}$ always assumes the state opposite the O-state.)

4-73 When power is first applied to the system, the turn-on preset circuit holds the PRESET inputs of the storage registers in the enabled (LO) state until 50msec after power is applied and drives the O output of each flip-flop to the HI state (the off-state of the five modes). To enable a particular mode, the corresponding control bit must be programmed to a logical 1. When the TME mode is programmed on, control bit $\overline{B04}$ = 0 (LO). The positive-going strobe pulse from amplifier Q2 transfers the LO level from the D-input to the O-output. Amplifier O3 inverts the Q-output, making TME = 1 (HI); the active state. TME is distributed to the timing mode flag circuits on logic and timing card A3 of each unit in the system.

4-74 The SYE mode is entered and stored in the same manner described for TME. The SYE output is taken from the $\overline{Q}$-side of its associated flip-flop and is a logical 1 (HI) when the mode is programmed on. SYE is routed through an interlock jumper on the input data plug to a two-stage amplifier (Q3 and Z17) on logic and timing card A3 and to the first 6941B unit in the system. The amplified SYE signal is wired to all output cards of the 6940B.

4-75 DTE is taken from the $\overline{Q}$-output of its associated flip-flop and is a logical 1 (HI) when the mode is programmed on. Amplifier Q6 inverts the HI level, making $\overline{DTE}$ = 0 (LO). $\overline{DTE}$ is wired to all accessory cards in the system but is utilized only by relay output cards, by TTL output cards, and by output cards having dual-rank storage.

4-76 ISL is taken from the $\overline{Q}$-output of its associated flip-flop and is a logical 1 (HI) when the mode is programmed on. The $\overline{Q}$-output is NANDed with the output of control word gate G1 and if a control word is not currently being programmed (ADDR = 1), the resulting LO output of gate G4 is inverted by O7 and is applied to amplifier Q9. Amplifier O9 inverts its input making $\overline{ISL}$ = 0 (LO). $\overline{ISL}$ is routed to the I/O selection gates on logic and timing card A3 and to all accessory card slots in the system. When applied to the I/O selection gates, $\overline{ISL}$ inhibits the input data bit path from the computer. Data bits from addressed input cards can now be returned to the computer on the return data bus.

4-77 Each time a control word address is issued, AND gate G4 is inhibited by $\overline{ADDR}$ = 0, making $\overline{ISL}$ = 1. The I/O selection gates will now pass the new programmed control word data to the unit select card. When the control word address is removed, the input data path from the computer will again be blocked provided the input select mode remained programmed.

4-78 IEN is taken from the $\overline{O}$-output of its associated flip-

flop and is a logical 1 (HI) when the mode has been programmed on. Amplifier Q10 inverts the HI level making $\overline{IEN}$ = 0 (LO). $\overline{IEN}$ is distributed to all accessory card slots in the system but is used only by input-type cards as an interrupt enable command. The Q-output of the IEN flip-flop is applied to and controls the state of the CTF flip-flop.

4-79 **CTF Generation.** Whenever the IEN mode is off, or is being programmed off by the current control word, a CTF flip-flop and associated delay circuit on the unit select card will generate a $\overline{CTF}$ signal. Any control word containing bit 8 = 0 (IEN mode on) will prevent this circuit from generating a $\overline{CTF}$ signal. A timing diagram showing how the unit select card $\overline{CTF}$ signal is generated (and inhibited) is given in Figure 4-6 and described in the following paragraphs.

4-80 If the IEN mode is off or is currently being programmed off, the clock pulse produced by the combination of DST and slot address 15 (control word tag) will strobe a HI level ($\overline{B08}$ = 1) into the IEN flip-flop. If the O output of the IEN flip-flop was already HI it will remain HI, and if it was LO (because IEN was previously on) it will switch HI. The clock signal is also applied to the CLR input of the CTF flip-flop. As long as the CLR input is at a HI level, the CTF flip-flop is allowed to store the data currently at its D-input when its clock terminal is strobed. (When the CLR input is LO, the O output is forced to a LO). The 8μsec delay circuit receives the clock output of gate G3. After an 8μsec delay from the start of the clock signal, the CLK input to the CTF flip-flop switches HI. This strobes in the HI level at the D input of the CTF flip-flop, setting the Q output HI. Amplifier O8 inverts this level making $\overline{CTF}$ LO. This flag signal is returned to the computer through the handshake flag circuit on the logic and timing card. The leading edge of $\overline{CTF}$ causes the computer to reset its gate input to the multiprogrammer. The gate resets DST which in turn resets the CLK and CLR lines in the unit select CTF circuit. The CLR line of the CTF flip-flop going LO resets $\overline{CTF}$ to a HI level.

4-81 When a control word containing an IEN mode selection is programmed, the output of the IEN flip-flop switches LO as soon as the clock pulse appears. The CLR line of the CTF flip-flop goes HI while the clock is present, allowing the CTF flip-flop to respond to the level at its D-input. Following an 8μsec delay, the CTF flip-flop is clocked and transfers the LO level at its D-input to the Q-output. The Q-output originally was LO (by the CLR line being LO) and thus there is no change in the output of the CTF flip-flop. The $\overline{CTF}$ output of the unit select card remains HI, not generating a flag.

4-82 The computer now awaits a $\overline{CTF}$ signal from an input card. All input cards received the interrupt enable command ($\overline{IEN}$) from the unit select card and the first input card to

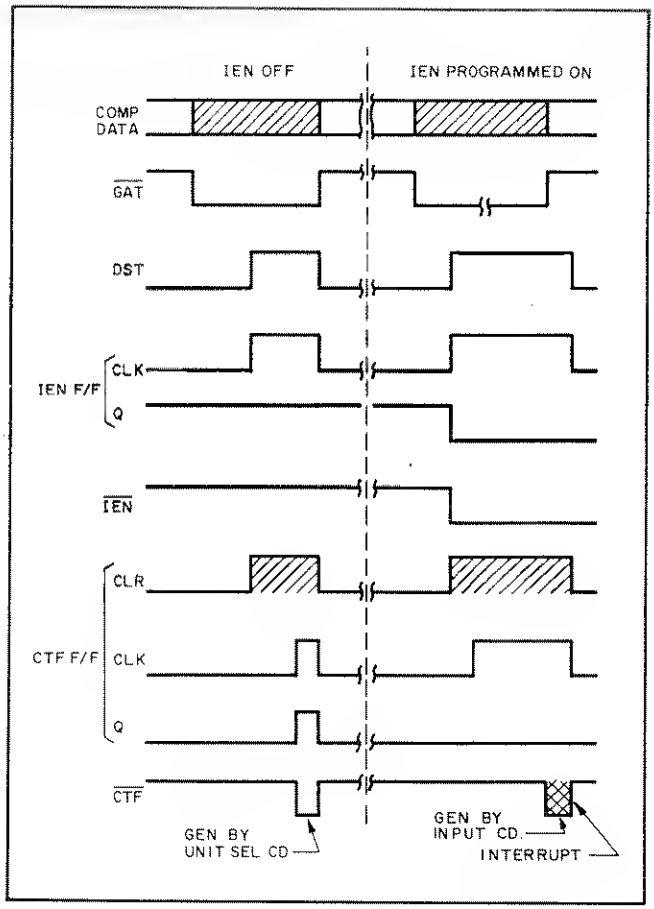


Figure 4-6. Unit Select Card CTF Generator, Timing Diagram

have valid input data available will set its $\overline{CTF}$ line LO. In response to the leading edge of $\overline{CTF}$, the computer will reset the gate input to the multiprogrammer. This resets $\overline{OST}$, which, on the input cards, resets $\overline{CTF}$. With IEN on, the trailing edge of $\overline{CTF}$ represents an interrupt request to the computer.

4-83 **Unit Address Logic.** The unit address logic consists of four D-type address storage flip-flops, a 1-of-16 address decoder, and 16 identical driver-inverters. Bits $\overline{B00}$, $\overline{B01}$, $\overline{B02}$, $\overline{B03}$ of control words represent programmed unit addresses. When a control word code is detected by gate G1, and a strobe signal is generated, the programmed unit address is stored in the four flip-flops of integrated circuit Z1. The flip-flop outputs are taken from the $\overline{Q}$-side of the flip-flops, thus generating the complement of the stored address bits. The stored address bits are applied to 1-of-16 address decoder Z2 which energizes one of its 16 output lines (drives it LO) according to the stored address. Driver-inverters A1 through A16 amplify and invert the unit-select output of the 1-of-16 decoder. The unit select lines are wired to the output card slots of the units identified by the U—— mnemonics.

4-84 Switch Register A11

4-85 Switch register A11 permits manual programming of the multiprogrammer system. It consists of 20 lighted pushbutton switches and associated programming logic. Sixteen of the switches (0 through 15) are used to develop data and control words, while the remaining four (LOAD OUTPUT, RETURN DATA, REMOTE/LOCAL, and CLEAR) select control functions.

4-86 The switch register is selected as the programming source when the REMOTE/LOCAL switch has been pressed to select the local mode (as indicated by the LED in its key cap being extinguished). With the local mode selected, the driver circuit sets LCL = 1 (HI) and $\overline{\text{LCL}}$ = 0 (LO). LCL enables the local programming gates while $\overline{\text{LCL}}$ is routed to remote/local selection card A2, where it inhibits the computer input data lines and enables the local data lines.

4-87 In address bit programming logic circuits M15 through M12, LCL is NORed with the debounced switch output. When both are in the LO-state, a positive-going pulse is generated and applied to the clock input of a D-type flip-flop. The flip-flop is connected in a toggling configuration ($\overline{\text{O}}$ connected back to D) so that each time the switch is pressed, the flip-flop is clocked and the O-output reverses state. The O-output of the flip-flop is NANDed with LCL and applied to remote local card A3 as M15 through M12. Data bit programming circuits M11 through MØØ operate in the same manner as the M15 through M12 circuits with one exception; LCL is NANDed with $\overline{\text{ISL}}$ and the resulting logic signal is NORed with the debounced switch outputs. This additional qualification insures that the last set of manually selected data will be preserved when an input mode (ISL) is programmed. When programming output functions in the LOCAL mode, the address bit outputs of the switch register (M15, M14, M13, and M12) are gated through the remote/local card and returned to LED drivers associated with bits 15, 14, 13, and 12 on the switch register. The manually-selected data bits are selected by the remote/local card, passed through I/O selection gates on the logic and timing card and then looped back through cables on the remote/local card to LED drivers associated with the data bits 0 through 12 on the switch register.

4-88 For locally programmed input functions (where $\overline{\text{ISL}}$ = 0), the address bits are generated, selected, and displayed in the same manner as for output functions, but the data bits are handled entirely differently. First, the local data bit programming logic circuits are disabled once ISL has been programmed on. Pressing bit switches 0 through 12 will produce no changes. Also, $\overline{\text{ISL}}$ inhibits the I/O selection gates on the logic and timing card and makes any addressed input card the source of data to be displayed on the 12 data bit switch register LEDs.

4-89 When REMOTE operation is selected, LCL = 0 (LO), driving M15 through MØØ to the HI-state; and $\overline{\text{LCL}}$ = 1 (HI), inhibiting the clear register circuit. The states of the toggled flip-flops are not affected when the mode is switched. In this way the last set of manually programmed data is stored and available when the LOCAL mode is again selected. In REMOTE operation, for output modes, the switch register LEDs indicate the input data from the computer; for input modes, the LEDs indicate the selected input card address and the data bits returned by the selected card.

4-90 **Power-On Initialize Circuit.** When the power is turned on, this circuit clears all of the data storage flip-flops. This presets the data register and ensures that the multiprogrammer is initialized to the remote mode. Switching to the local mode causes an LED check to be made. This circuit also ensures that if the line voltage fluctuates, the multiprogrammer always resets when the proper line voltage is re-established.

4-91 **Clear Register Circuit.** When the CLEAR switch is pressed, all manual bits are cleared to the 0-state. The clear register circuit combines the debounced output of the CLEAR switch and the $\overline{\text{LCL}}$ line, NANDing them so that the CLEAR switch functions only in the local mode. Pressing the CLEAR switch sets the O outputs of the bit flip-flops to the HI state, thus clearing all bits. The indicator LED in the CLEAR switch is directly connected across 5Vdc and is always on.

4-92 **Load Output Circuit.** When the LOAD OUTPUT switch is pressed, an LDO pulse is generated which loads the manually-programmed data into the multiprogrammer. Pressing the LOAD OUTPUT switch produces a LO output from the driver. The output is then NANDed with LCL. If the LOCAL mode has been selected, the NAND gate output switches from the LO- to the HI-state and this level is coupled to remote/local card A2 as LDO. The remote/local card inverts LDO to become gate pulse $\overline{\text{GAT}}$. The $\overline{\text{GAT}}$ pulse is returned to the LED driver associated with the LOAD OUTPUT switch and turns on the LED for as long as the switch is pressed.

4-93 **Return Data Circuit.** The return data circuit generates a positive output pulse when the RETURN DATA switch is pressed. In the LOCAL mode, this pulse (RDA) replaces the flag normally generated by logic and timing card A3. The RETURN DATA LED will indicate the presence of either of two signals. For output modes, the LED will indicate the presence of a flag signal. For input modes, it will light when an addressed input card returns an IRO signal. Circuit operation is identical to the LOAD OUTPUT circuit.

4-94 Typical Output Card

4-95 A typical output card consists of a slot address gate circuit, data storage registers, a data conversion circuit, and a timing flag generator circuit. The typical output card shown in Figure 7-2, Sheet 2, is located in slot 400. When slot 400 is addressed, $\overline{B15}$, $\overline{B14}$, $\overline{B13}$, and $\overline{B12}$ are all HI. If unit Ø has been selected by a previous control word, U**ØØ** is also HI. When DST appears, a positive strobe pulse is generated and applied to data storage flip-flops and the timing flag pulse generator circuit. The strobe pulse enters data bits $\overline{B00}$ through $\overline{B11}$ into local storage. The digital output of the storage flip-flops is converted to an equivalent resistance, voltage, or digital output and applied to the user's system.

4-96 The timing flag pulse generator produces a $\overline{CTF}$ pulse that starts at DST and lasts until a timing capacitor within the generator times-out.

4-97 Typical Input Card

4-98 A detailed block diagram of a typical TTL input card is shown in Figure 7-2, Sheet 2. The diagram does not show the many jumper options available on the input card which permit logic sense inversions of the data bit and flag inputs from the external device and logic sense control of the gate output to the external device. Other jumper options on the card allow either the leading or the trailing edge of the external device flag to reset the gate flip-flop and set the flag flip-flop. All these options are covered in detail in the 69431A Instruction Manual for the TTL input card. In this discussion it will be assumed that the leading edge of the device flag resets the gate flip-flop and the trailing edge of the device flag sets the flag flip-flop.

4-99 The typical input card is comprised of two circuit groups. One group buffers, stores, and gates-through 12-data bits from the external device. The second circuit group implements gate-flag transfers between the external device and the multiprogrammer. The circuit operation will be described for the two basic input modes; dedicated, and interrupt-search.

4-100 **Dedicated Input Timing Mode.** The dedicated input mode is programmed in two steps: (1) programming a control word with ISL = 1, IEN = 0, and TME = 1; (2) programming the desired card address and issuing a computer gate signal.

4-101 The first step does not immediately affect the input cards. It simply turns the 12-data bit lines in the direction of the computer, enables the CTF return path to the computer, and makes the $\overline{ISL}$ input to the input cards true. In the second step, the address of the desired input card is programmed, along with a computer gate. When the address gate on the selected input card is enabled, it allows the 12 input-data NAND gates to pass the current contents of the 12 data storage registers to return data lines $\overline{B00}$ through $\overline{B11}$. (The computer should not immediately accept this data.)

4-102 The input card arming logic examines the states of $\overline{ISL}$, ADDR, and DST, and when all three are true (as they now should be) it sets a gate flip-flop and a control flip-flop on the card. The Q-output of the gate flip-flop does two things: (1) it sends a gate ($\overline{GATE}$) signal to the external device and, (2) it resets the flag flip-flop. The $\overline{Q}$ output of the flag flip-flop is NANDed (by gate G1) with ADDR and since both are true the NAND gate output goes LO, switching $\overline{CTF}$ to the busy state. When the external device returns the leading edge of its flag, the edge is detected and causes a negative pulse ($\overline{FLL}$) to be generated which resets the gate flip-flop. The card remains in this state ($\overline{CTF}$ busy) until the external device signals, via the trailing edge of its flag, that it has data ready. The trailing edge is detected and negative pulse $\overline{FLT}$ is generated. This pulse clocks the input data storage registers which accept and store the new data from the external device, and it sets the flag flip-flop. The $\overline{Q}$-output of the flag flip-flop switches LO, inhibiting NAND gate G1. The $\overline{CTF}$ line now returns to the ready state, signaling the computer to accept the new data on the return data lines.

4-103 **Interrupt Search Mode (jumper W6 out).** Four programming steps are involved in the interrupt-search mode.

Step 1. Establish initial mode conditions by programming a control word with ISL = 1, IEN = 0, and TME = 0.

Step 2. Arm desired input cards by programming card addresses. (A computer gate must accompany each address as it is programmed.)

Step 3. Select the interrupt enable mode by programming a control word with IEN = 1, TME = 1, and ISL = X (X = doesn't care).

Step 4. Wait for the multiprogrammer flag to indicate that one or more addressed input cards has valid data ready. Then, poll the input cards (by issuing their addresses) in a software determined order. Do not issue a computer gate while polling. Examine bit 15 of each return data word in the computer and accept the data only when bit 15 = 1. (The state of bit 15 is determined by IRQ from the addressed input card; when the addressed input card has valid data available, IRQ makes bit 15 = 1.)

4-104 Step (1) reverses the data bit lines, turns off the timing mode, and sets up an arming condition ($\overline{ISL}$ = 0).

4-105 In Step (2), the card is armed in the same manner described for the dedicated input mode, but since the timing mode is off, $\overline{CTF}$ has no effect on the return flag to the computer. When the device returns the trailing edge of its flag to the input card (indicating data ready) it will set the

flag flip-flop and strobe new data into the card's input data bit storage registers. The card will now wait, with its flag flip-flop set and new data in its storage registers, for the interrupt mode to be programmed.

4-106 In Step (3) IEN and TME are both programmed on. A computer gate must accompany the control word as it is issued. A handshake flag is normally generated by the unit select card when a control word is programmed, but when the control word contains an IEN mode selection, the flag is inhibited. The computer must now wait, with its gate line set, for a CTF flag from an input card. When the computer receives this flag it should start an interrupt request.

4-107 On all input cards, NAND gate G2 implements the function $\overline{DST \cdot IEN \cdot CONT \cdot FLAG}$. This function determines the state of the $\overline{CTF}$ line in the interrupt mode. DST·IEN·CONT will be true on all cards that have been armed. If the flag flip-flop on the card has been set (indicating data ready), the FLAG function will also be true. Thus, when all four functions are true, the $\overline{CTF}$ line is set to the busy state. When the computer notes this ready-to-busy transition of the $\overline{CTF}$ line it resets its gate, which resets DST. With DST off (LO) NAND gate G2 is inhibited, returning the $\overline{CTF}$ line to the ready state. This latter transition of $\overline{CTF}$ represents the actual interrupt request.

4-108 The computer should now poll the input cards and pick up data from the cards which have their flag flip-flop set.

4-109 Polling is done is a predetermined order by programming the card address without a computer gate. Keeping the computer gate false prevents the input cards from being re-armed as they are addressed.

4-110 As each input card is addressed, it will pass its 12 data bits onto the return data lines. At the same time, the $\overline{IRQ}$ output of the addressed card will be true (LO) if the card's flag flip-flop has been set. As previously stated, $\overline{IRQ}$ directly controls $\overline{B15}$ for input modes, and when $\overline{IRQ}$ is true (LO) so is $\overline{B15}$ (LO). The computer should accept the return data word when $\overline{B15}$ is true.

4-111 An input card should not be left with its control and flag flip-flop set after it has been serviced. It should either be re-armed (so that a new gate is sent to the external device) or disarmed (control flip-flop reset) by programming ISL off and addressing the card, along with a computer gate.

4-112 **Interrupt-Search Mode (jumper W6 in).** This mode is similar to the interrupt search mode with W6 out, the main difference being that card arming and interrupt enable are done in one step. The first card with new data available will request the interrupt. There are two qualifications on generating a gate to the external device using IEN, as expressed in the equation, $\overline{IEN \cdot CONT \cdot FLAG}$. This equation simply states that IEN is allowed to initiate a gate except when the control flip-flop is already set or when the flag flip-flop is in the middle of an operation.

4-113 DETAILED CIRCUIT ANALYSIS

4-114 This paragraph contains a detailed analysis of all discrete-component circuits of the 6940B Multiprogrammer on a card-by-card basis. Those circuits whose operation is obvious (such as single-stage amplifiers and termination networks) are not covered in detail. Detailed descriptions of the 6940B logic circuits are provided in the detailed block diagram discussion.

4-115 Input Card A1

4-116 Input card A1 contains 17 identical resistive termination networks and a pull-up resistor for the $\overline{FLA}$ return line to the computer.

4-117 Remote/Local Card A2

4-118 Remote/local card A2 performs data selection functions as described in Paragraph 4-46. A jumper option on A2 selects either +5 or +12V. The jumper selected voltage is also coupled through cable W2 to data-bit buffer amplifiers on card A3. The flag stretcher circuit following gate G34 maintains the minimum duration of the $\overline{FLA}$ output at 20μsec.

4-119 Logic and Timing Card A3

4-120 Logic and timing card A3 (Figure 7-2, Sheet 1) contains two circuits that require detailed circuit analysis. They are the data strobe generator and the handshake flag generator. A timing diagram for these circuits is given in Figure 4-7.

4-121 **Data Strobe Generator.** The data strobe generator consists of a 2μsec delay circuit and related amplifiers.

4-122 The $\overline{GAT}$ input signal from remote/local card A2 is inverted twice, by Z3, and appears at the input to the 2μsec delay circuit in the same logic sense as the original $\overline{GAT}$ pulse. Before the computer sets $\overline{GAT}$ to the LO state, capacitor C5 is charged to approximately +3.5 volts through diode

CR1, holding Z3-8 LO. This LO logic level is inverted twice, by Z7 and Q9, thus holding the DST line at 0 volts.

4-123 When the computer sets the $\overline{GAT}$ line LO, capacitor C5 starts to discharge toward 0 volts through R22. After approximately 2μsec, C5 has discharged to less than 0.9 volts, the threshold voltage of Schmitt trigger input Z3-9. The resulting HI logic level at Z3-8 is again inverted twice setting the DST line HI. When the computer resets $\overline{GAT}$ to the HI state, capacitor C5 charges rapidly through CR1, returning DST to the LO level.

4-124 **Handshake Flag Generator.** The handshake flag generator consists of an 8μsec delay circuit and associated NAND gate. This circuit adds an additional 8μsec delay to the 2μsec delay so that the handshake flag starts 8μsec from the start of DST and 10μsec from the start of $\overline{GAT}$. Before $\overline{GAT}$ is set LO by the computer, the voltage at Z7-3 is HI. Capacitor C6 is charged positively through CR2 making Z3-2 LO. This LO inhibits NAND gate G12.

4-125 Following a 2μsec delay from the time $\overline{GAT}$ goes LO, the voltage at Z7-3 also goes LO. Capacitor C6 starts discharging through R23 and after approximately 8μsec, the voltage across C6 is sufficiently LO to drive Schmitt trigger output Z3-2 HI. This HI is logically NANDed with U00 (HI if unit 0 is selected) and the output of the timing mode flag circuit (HI if TME is off). If all the conditions for generating a handshake flag are present, the output of NAND gate G12 will go LO causing the $\overline{FLG}$ line to go LO. When $\overline{GAT}$ is reset, the 8μsec delay circuit and $\overline{FLG}$ are also reset.

4-126 Unit Select Card A5

4-127 In addition to the logic circuits, which were described previously, unit select card A5 (Figure 7-2, Sheet 1) contains several single-stage driver-inverters and a turn-on preset circuit. Only the turn-on preset circuit requires a detailed description.

4-128 **Turn-on Preset Circuit.** This circuit holds the direct preset input of the mode storage registers in the LO state for 50msec after power is first turned on, clearing them to the inactive state (Q = HI).

4-129 When power is turned on, +5 volts is applied across the R-C circuit consisting of resistors R17 and R18 and capacitor C11. Since C11 cannot charge instantaneously, the base of Q5 remains below +5 volts, switching Q5 on. As the collector voltage of Q5 goes positive, Q4 is turned on, driving the preset line of the storage register LO. When capacitor C11 has charged to +3.8 volts (in approximately 50msec) both Q5 and Q4 are cut off, returning the direct preset line to the HI state. Diode CR1 provides a rapid discharge path for C11 when power is turned off.

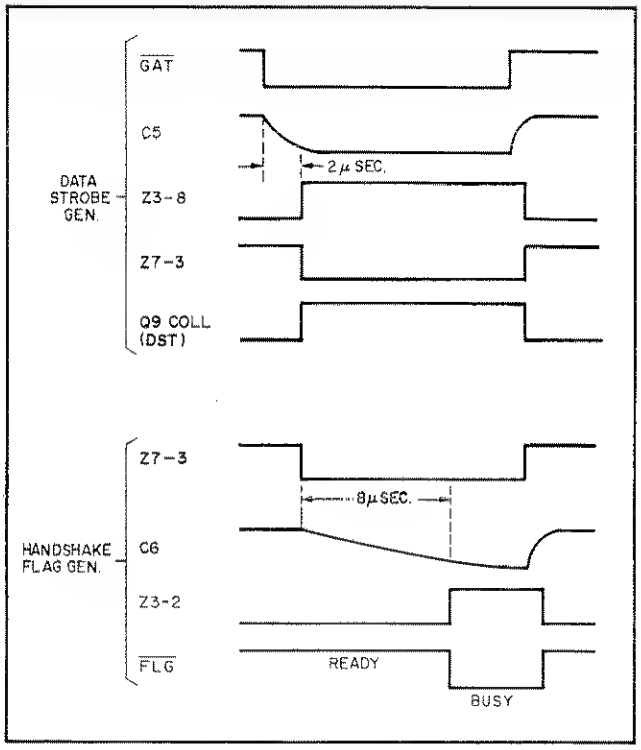


Figure 4-7. Logic and Timing Circuits, Timing Diagram

4-130 Main Power Supply Board A10 (See Figure 7-2, Sheet 4)

4-131 The main power supply board consists of a +5 volt regulator, four separate ±20 volt rectifier-filters, a +12 volt rectifier-filter, and a −12 volt rectifier-filter. The selected ac input power (100, 120, 220, or 240Vac) is applied to the rectifier-filters via power transformer T1 and the A12 power module (see Section II). The main power fuse F1 (4A for 100/120Vac or 2A for 220/240Vac) is located in A12. A 10A fuse (F2) is in the +12 (unreg.)/+5V (reg.) rectifier-filter circuit and a 0.75A fuse (F3) is in the −12V (unreg.) rectifier-filter circuit. Operation of the rectifier-filter circuits is obvious from inspection of the schematic diagram. The +5 volt regulator is described in the following paragraphs.

4-132 **Regulator Circuit.** The voltage regulator portion of the +5 volt supply consists of comparison amplifier U1, driver Q5, and series regulators Q1 and Q2. Comparison

amplifier U1, (inverting input) senses the regulated +5V output via a remote sense wire connected to slot 300 (A9J300, pin C). The remotely sensed voltage is compared with a reference voltage which is applied to the non-inverting input of U1. The reference voltage is obtained from a reference zener diode (temperature compensated) inside the U1 package. The output of U1 controls the conduction of driver Q5. The collector current of Q5 is then used to control the conduction of series regulators Q1 and Q2 which in turn control the level of the output voltage. If the voltage at A9J300-C attempts to increase from a preset level (nominally +5 volts) the conduction of Q5 will decrease causing both series regulators Q1 and Q2 to decrease conduction. The voltage drop across the series regulators will thus increase and return the output voltage at A9J300-C to +5 volts. A decrease in output voltage will cause Q1, Q2 and Q5 to conduct more heavily and increase the output voltage to +5 volts.

4-133 Capacitor C16 provides frequency compensation; capacitor C15 and resistor R20 provide loop stabilization. Diodes CR23 and CR24 limit the maximum input to the amplifier protecting it against excessive voltage excursions. Potentiometer R18 permits adjustment of the output voltage.

4-134 **Current Latch Circuit.** The current latch circuit is made up of overcurrent detector Q3, current latch Q4, and current latch amplifier Q6. The circuit monitors load current by sensing the voltage drop across resistor R4. If the load current increases to overload proportions (nominally 6.5 amperes) the voltage drop across R4 increases to 1.10 volts, which is sufficient to bias-on overcurrent detector Q3. Detector Q3 and current latch Q4 are connected in a regenerative feedback loop so that once Q3 is turned on it is latched in that state by Q4. With Q3 saturated, the base and emitter voltages of Q4 become more positive. The positive-going-emitter voltage switches on current latch amplifier Q6, which effectively short circuits the base-emitter junction of driver amplifier Q5. This switches off Q1, Q2, and Q5, reducing the output voltage to less than +1 volt. The regulator will remain in this state until LINE switch S1 is switched OFF, the overload condition is removed, and S1 is switched ON again.

NOTE

Wait at least 10 seconds for the latch circuits to discharge before resetting (turning S1 back on) the unit.

4-135 **Overvoltage Crowbar Circuit.** This circuit consists of zener diode VR2, overcurrent detector Q7, and SCR crowbar CR26. While the output voltage remains below +6.2V nominal, overvoltage detector Q7 is biased off, as is CR26. If the output voltage becomes greater than +6.2 volts, the voltage drop across R24 rises above +0.7 volts. This causes Q7 to conduct and fire the SCR. The short circuit produced by the SCR forces the regulator into current latch, reducing the voltage output to less than +1 volt. Capacitor C18 reduces noise susceptability of the SCR triggering circuit. The unit must be turned off and then on in order to reset the overvoltage crowbar circuit.

4-136 Switch Register Board A11

4-137 Switch register board A11 (Figure 7-2, Sheet 3) contains five different IC circuits. These are described in the following paragraphs.

4-138 **Switch Contacts and Debounce Circuitry.** When the multiprogrammer is in the local mode, the pushbutton switches on the front panel are used to program bit patterns manually. To ensure stable 0 and 1 logic levels when activating a pushbutton, each switch is buffered from the logic circuitry by a contact bounce eliminator circuit contained in IC Z16, 18, 19, or 24. These ICs block extraneous level changes that result when interfacing to mechanical contacts. The ICs eliminate the effects of contact bounce by delaying the digital output for four clock periods after the switch contact has stabilized. An external capacitor sets the operating frequency of the internal R-C oscillator used to clock each IC package.

4-139 **LED Drivers.** The 20 LED drivers are non-inverting buffers that sink the cathode of an LED when the control line from the remote/local card goes to the 0-state (LO).

4-140 **Remote/Local Flip-flop.** The remote and local modes are alternately selected by pressing the REMOTE/LOCAL switch. A pulse from the REMOTE/LOCAL switch toggles a J-K flip-flop. The flip-flop's $\overline{Q}$ output is inverted once to provide the LCL control line and then inverted again to provide the $\overline{\text{LCL}}$ signal transmitted to the remote/local card. In the local mode, the LCL signal enables the local select output gates, and the $\overline{\text{LCL}}$ signal disables the data lines from the computer.

4-141 **Local Data Storage Flip-flops.** These flip-flops temporarily store bit patterns manually entered through the switch register. NOR gates at the flip-flop inputs and NAND gates at their outputs disable all of them unless in the local mode. Data bits 0 through 11 are also disabled when in the input mode.

4-142 Each NOR gate output is connected to a flip-flop's clock input, and the flip-flop's $\overline{Q}$ output is connected to its D input. This configuration causes the Q output to toggle with each pulse received from the debounce circuit. Once the LED indicators show the flip-flops contain the desired data, an entry can be gated in by depressing the LOAD OUTPUT swtich.

4-143 **Power-On Initialize Circuit.** This circuit is a combination undervoltage detector and delayed power-on reset circuit. The undervoltage detector consists of a comparator, a resistive divider, and a voltage reference. The delay is provided by an R-C network at the comparator output and a switch debounce circuit. The switch debounce circuit ensures a sharp transition for the TTL buffers that initialize the local data storage flip-flops. The remote/local flip-flop is initialized to the remote mode, and the 16 data bit flip-flops are initialized to all ones. (All 16 data bit LEDs light on first switching to the local mode).

4-144 As power is first applied to the circuit, the reference input provided by the stabistor diode (a nominal 2V reference) is higher in potential than the input from the resistive divider, causing the comparator output to be LO. The comparator output clamps timing capacitor C13 at zero volts and holds the flip-flops in their initialized state. As the 5V supply reaches approximately 4 volts, the comparator output switches HI, allowing C13 to charge through the pull-up resistor in the debounce circuit. The flip-flop's clear inputs are held LO until the voltage on C13 reaches the switching threshold of the debounce circuit.

4-145 If the supply voltage should dip to about four volts during the operation, the flip-flops will be initialized again, assuring that the multiprogrammer always powers up in the remote mode.

4-146 Output Adapter Card A8

4-147 Output adapter card A8 (Figure 7-2, Sheet 2) routes the data bits, address bits, 15 unit selection lines, and the mode and timing signals from the multiprogrammer backplane (A9 interconnect board) to output connector J2. The A8 card includes buffer amplifiers for the 15 unit selection lines and the SYE and TME signal lines. The data bits, address bits and the other signal lines are buffered on 6941B multiprogrammer extender unit number 01.